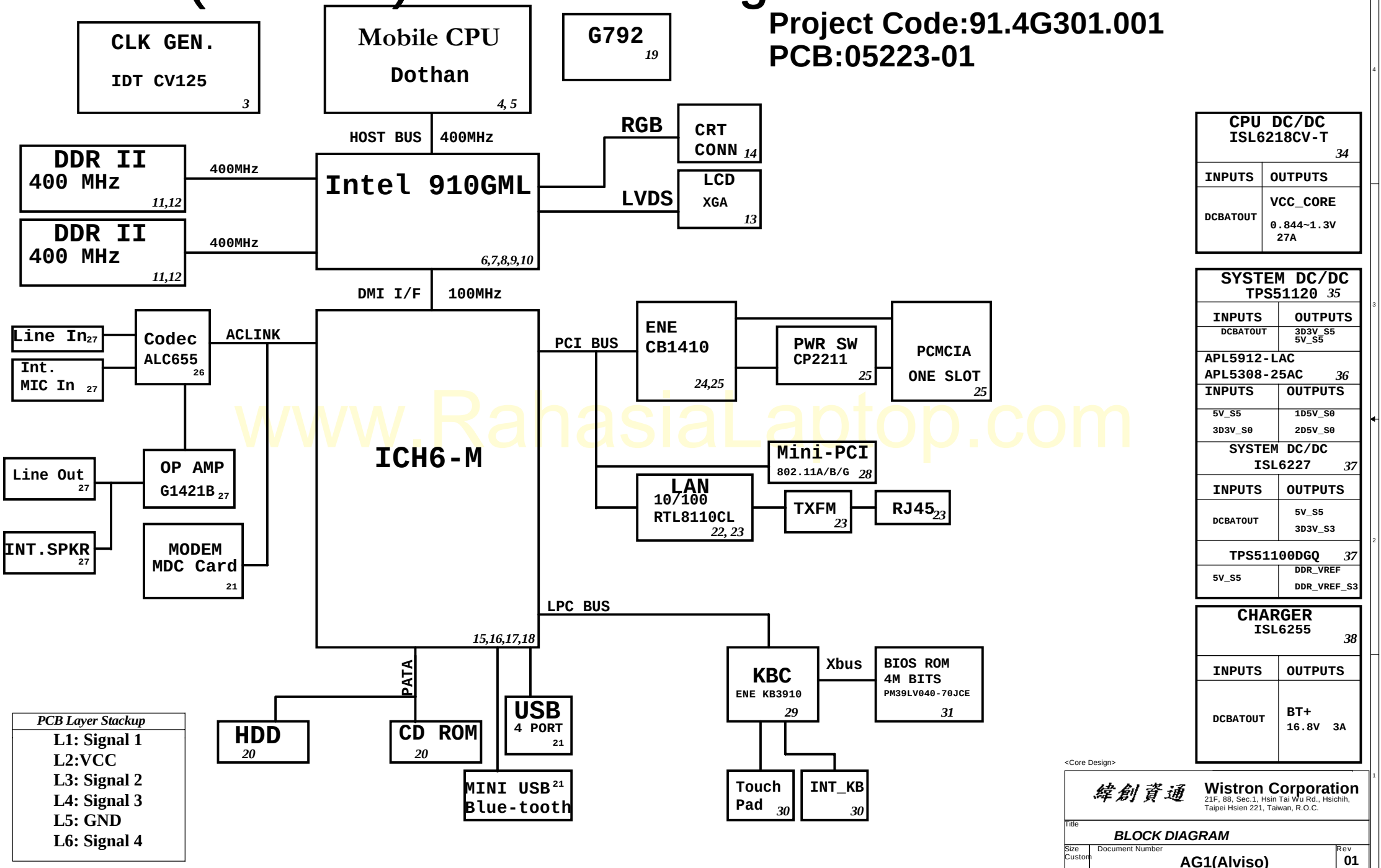
AG1(Alviso) Block Diagram 2005/11/01

Project Code:91.4G301.001
PCB:05223-01



CPU DC/DC
ISL6218CV-T *34*

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC
TPS51120 *35*

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

APL5912-LAC
APL5308-25AC *36*

INPUTS	OUTPUTS
5V_S5 3D3V_S0	1D5V_S0 2D5V_S0

SYSTEM DC/DC
ISL6227 *37*

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3

TPS51100DGQ *37*

INPUTS	OUTPUTS
5V_S5	DDR_VREF DDR_VREF_S3

CHARGER
ISL6255 *38*

INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

PCB Layer Stackup

L1: Signal 1
L2:VCC
L3: Signal 2
L4: Signal 4
L5: GND
L6: Signal 4

<Core Design>

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Title: *BLOCK DIAGRAM*

Size: Custom | Document Number: AG1(Alviso) | Rev: 01

Date: Tuesday, November 01, 2005 | Sheet 1 of 40

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

PCI Routing

	IDSEL	IRQ	REQ/GNT
1410	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

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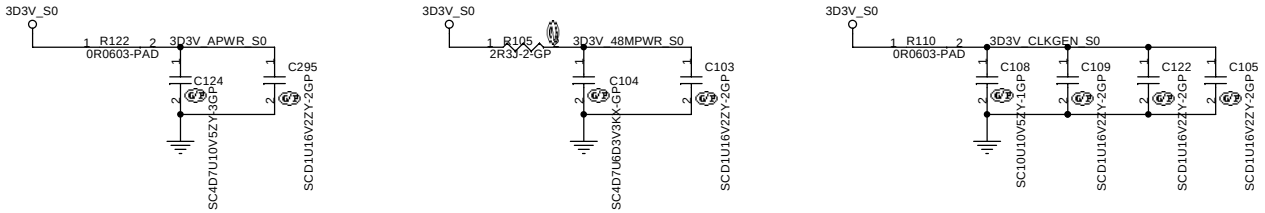
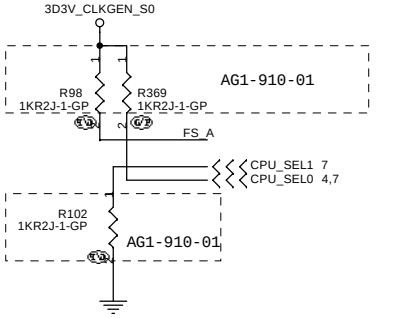
Title: *Memo*

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

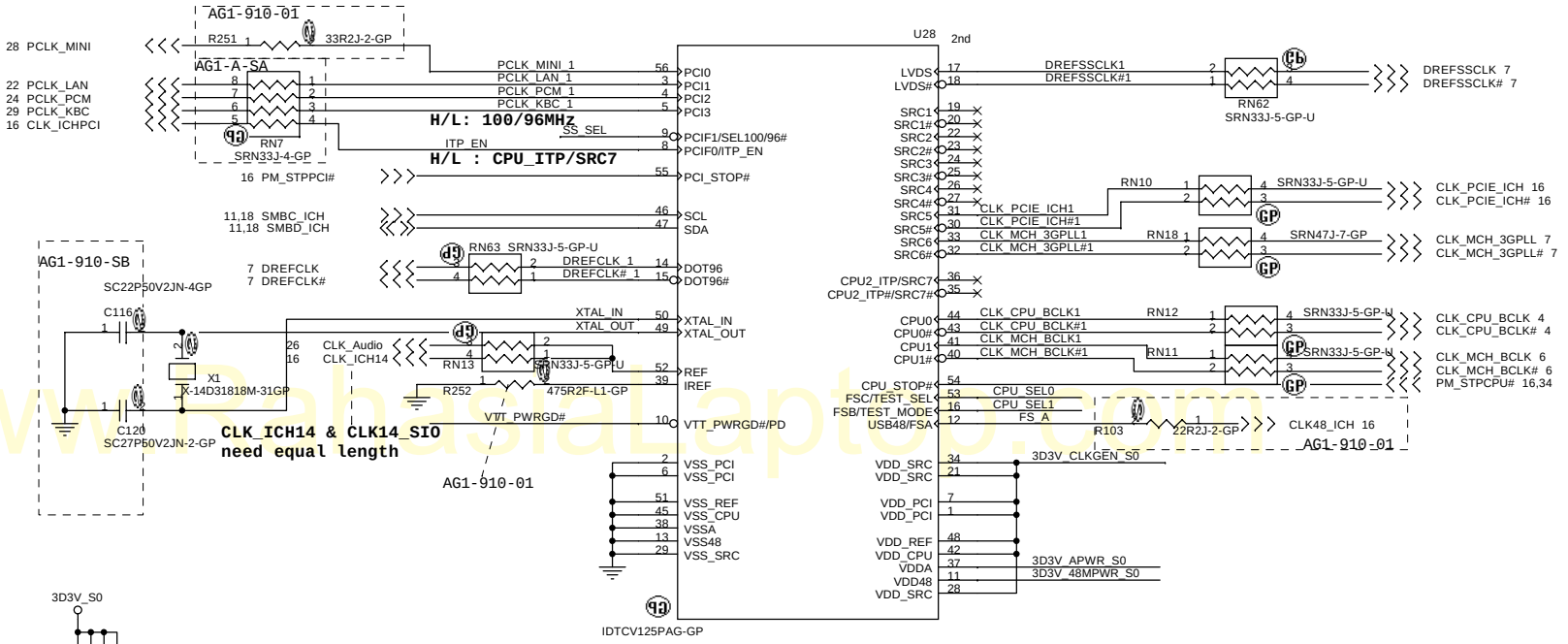
Date: Tuesday, November 01, 2005 | Sheet 2 of 40

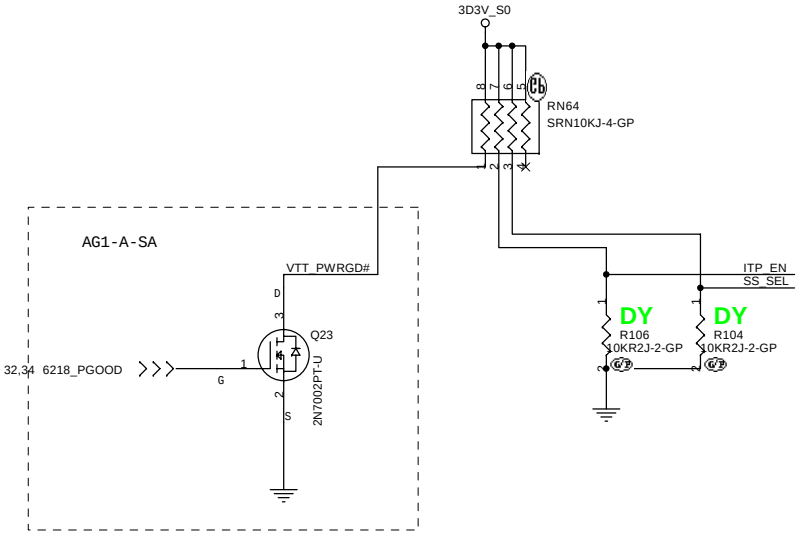


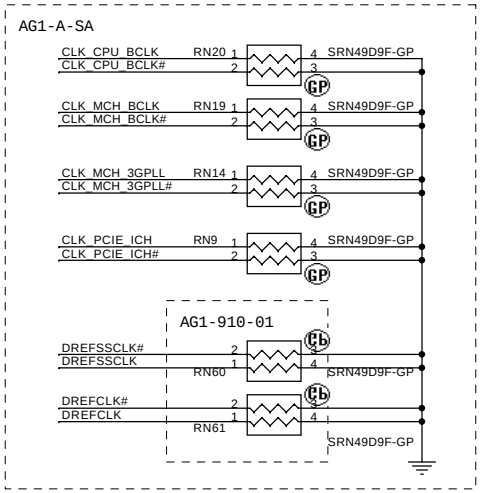
IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

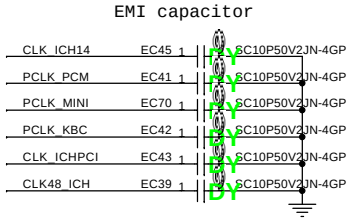


FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved









<Core Design>

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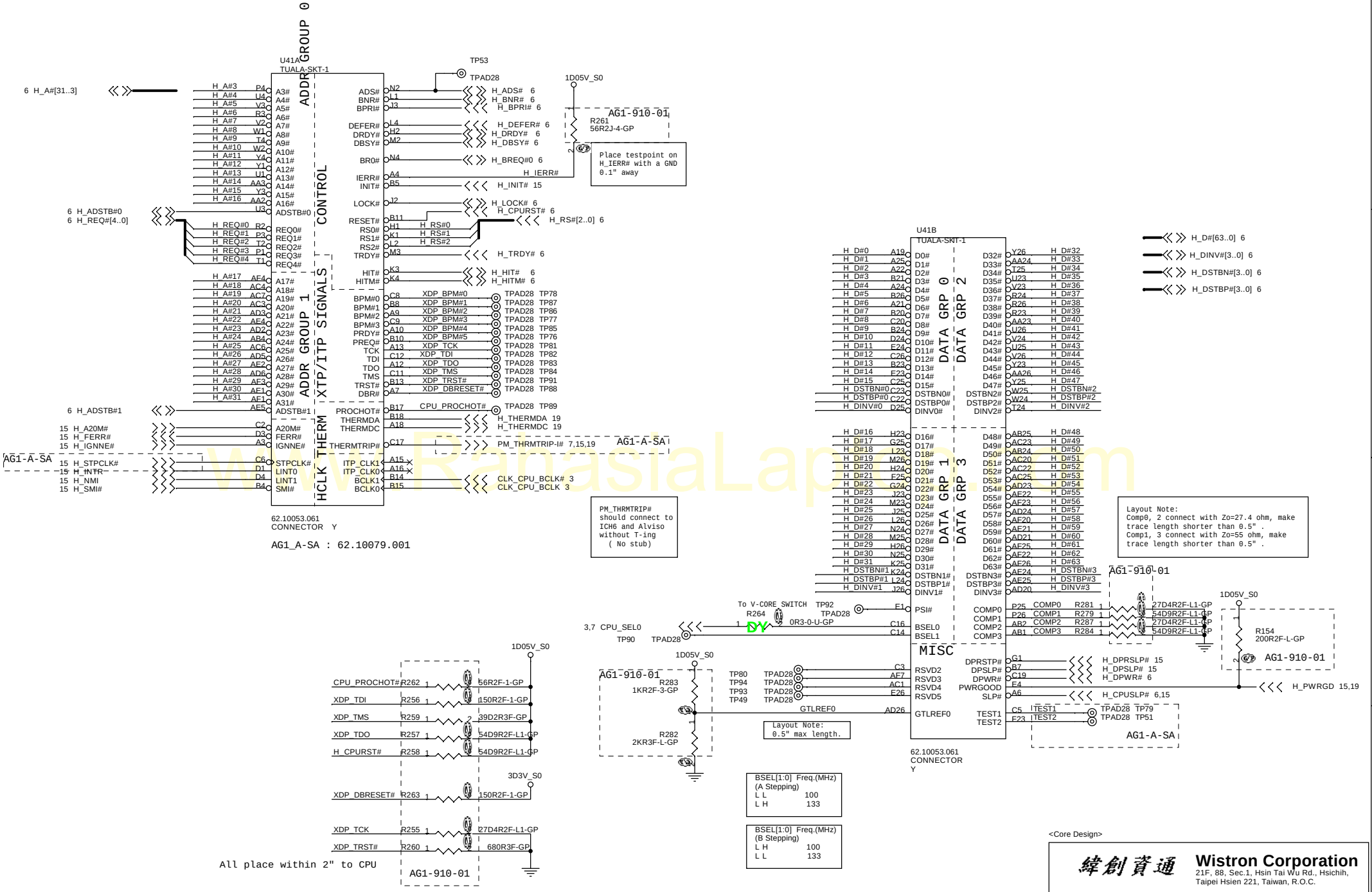
Title: ***Clock Generator - IDT125***

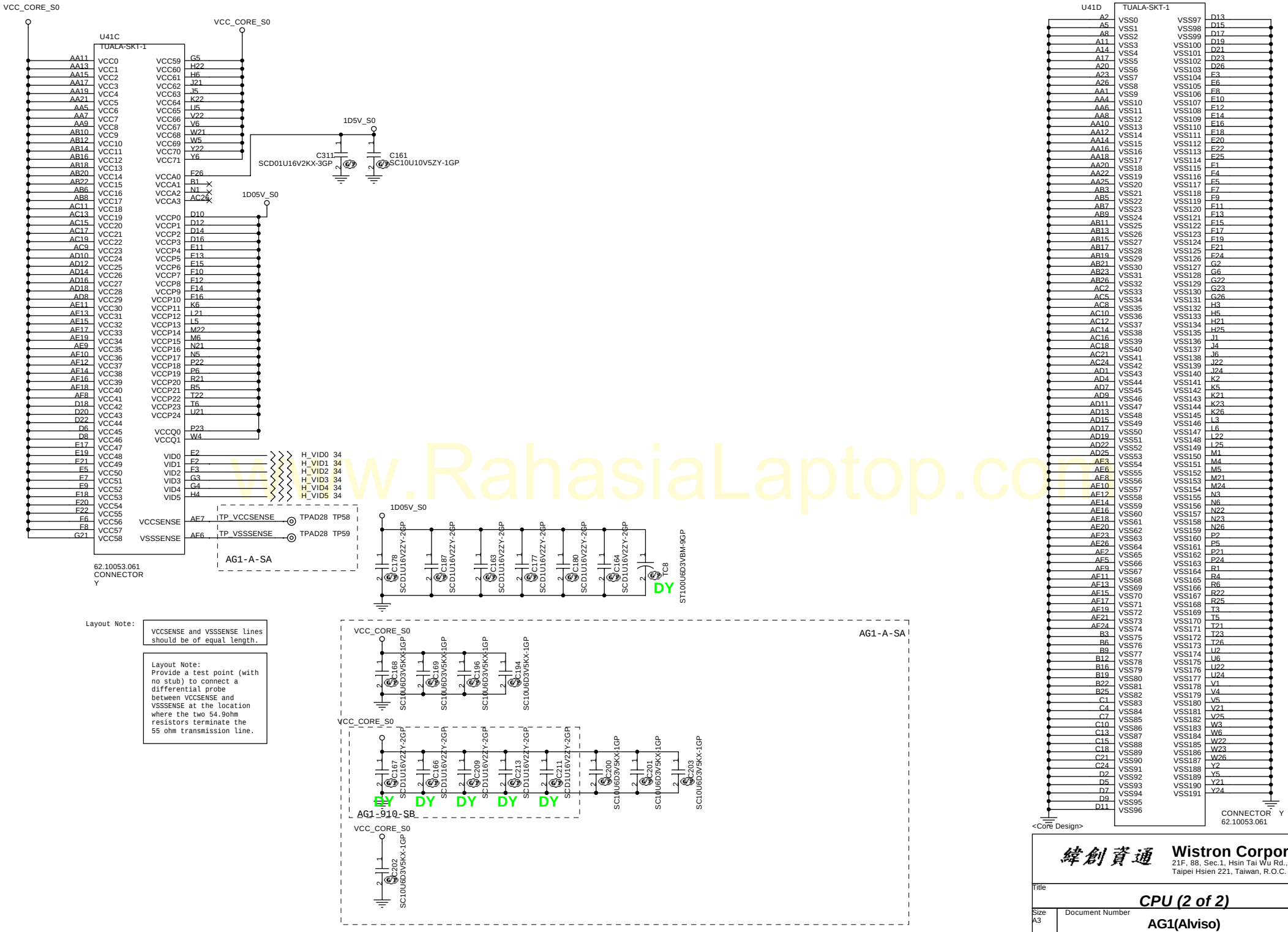
Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Friday, October 28, 2005 Sheet 3 of 40



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU (1 of 2)***
Size A3	Document Number **AG1(Alviso)** Rev **01**
Date: Monday, October 31, 2005	Sheet 4 of 40



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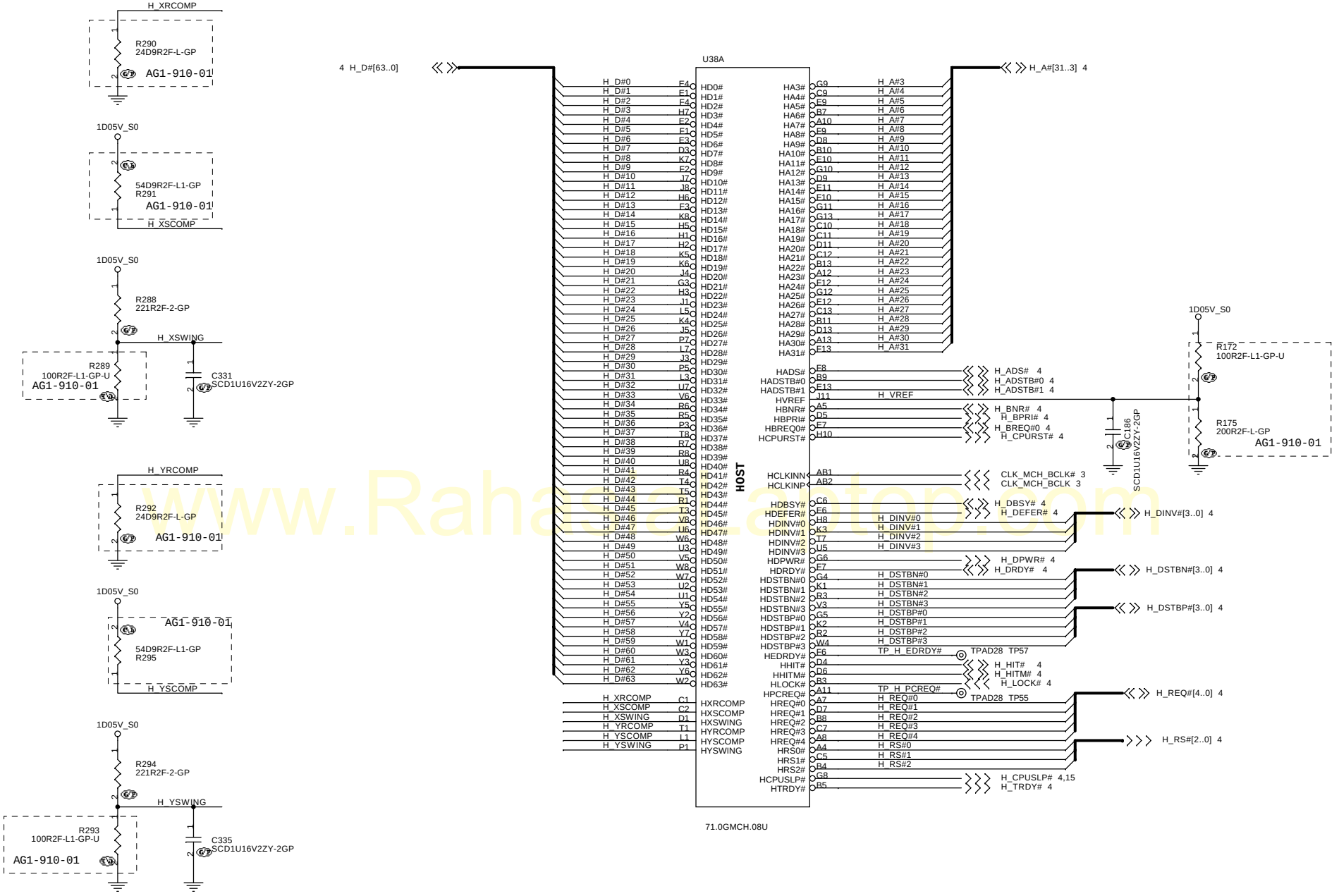
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (2 of 2)***

Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Monday, October 17, 2005 Sheet 5 of 40



Place them near to the chip

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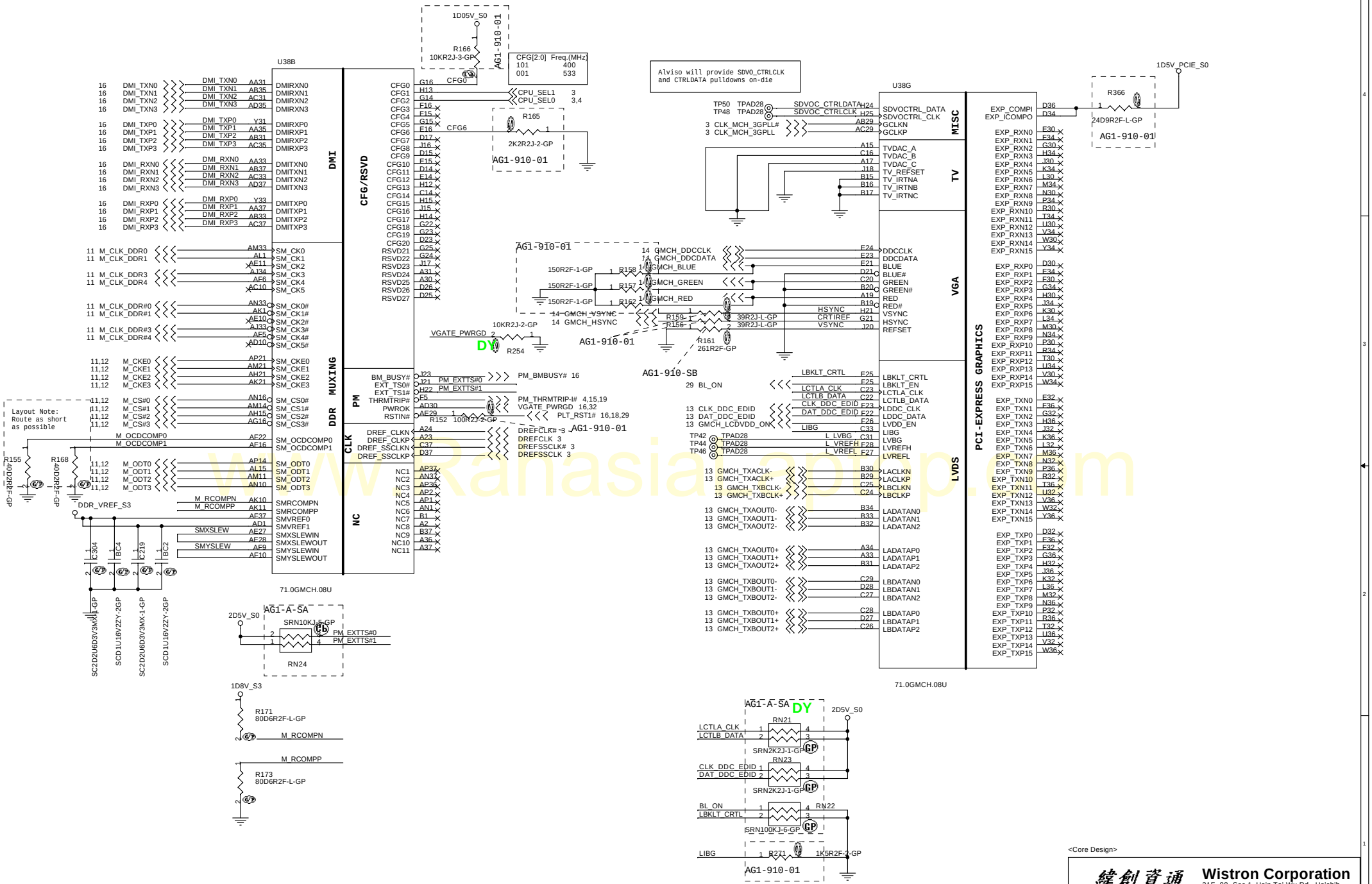
Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	**AG1(Alviso)**	**01**

Date: Tuesday, October 25, 2005 Sheet 6 of 40


U38B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
U38G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
Layout Note: Route as short as possible
DDR_VREF_S3
71.0GMCH.08U
AG1-A-SA
AG1-910-01
AG1-910-SB
1D05V_S0
1D05V_PCIE_S0
2D5V_S0
1D8V_S3
CFG[2:0] Freq.(MHz)
101 400
001 533
<Core Design>
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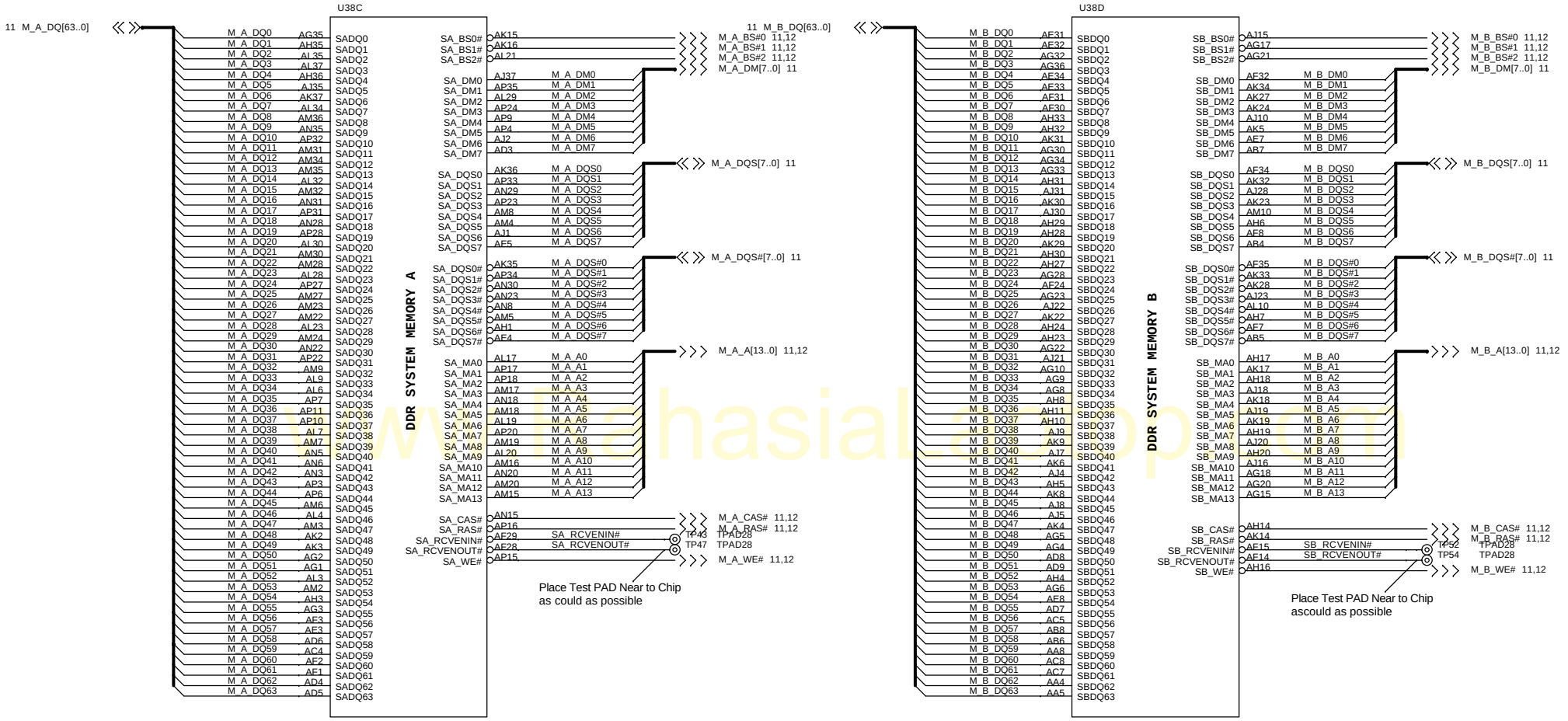
GMCH (2 of 5)
AG1(Alviso)
01
Tuesday, October 25, 2005
Sheet 7 of 40



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緯創資通 **Wistron Corporation**
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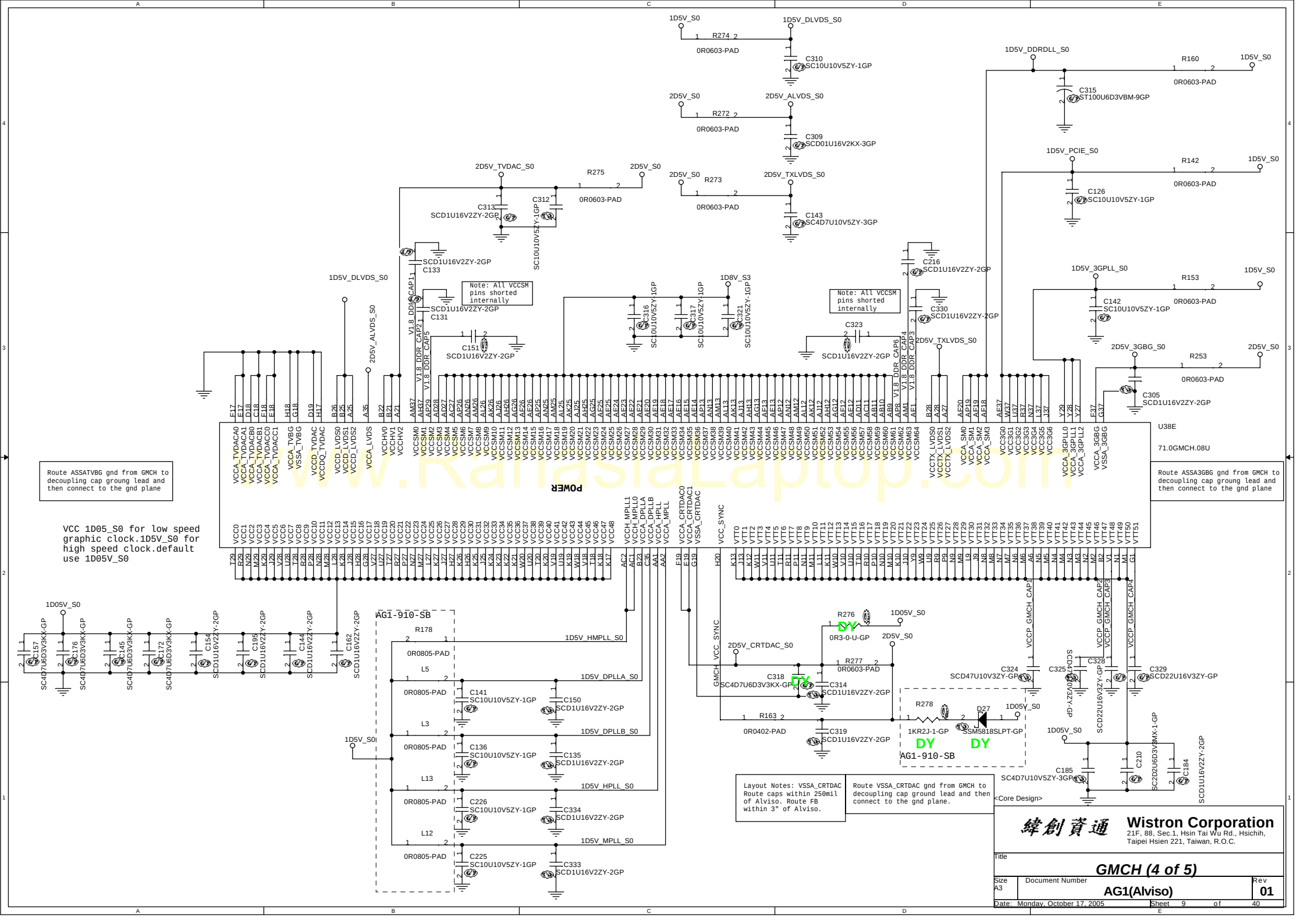
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (3 of 5)**

Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Monday, October 17, 2005 | Sheet 8 of 40


1D5V_S0
1D5V_DLVDS_S0
R274
0R0603-PAD
C310
SC10U10V5ZY-1GP
1D5V_DDRDLL_S0
R160
C315
ST100U6D3VBM-9GP
2D5V_S0
2D5V_ALVDS_S0
R272
C309
SCD01U16V2KX-3GP
1D5V_PCIE_S0
R142
C126
2D5V_TVDAC_S0
R275
C313
SCD1U16V2ZY-2GP
C312
SC10U10V5ZY-1GP
2D5V_TXLVDS_S0
R273
C143
SC4D7U10V5ZY-3GP
C133
1D5V_3GPLL_S0
R153
C142
1D8V_S3
C316
C317
C321
C216
C330
C323
2D5V_3GBG_S0
R253
C305
SCD1U16V2ZY-2GP
C131
C151
Note: All VCCSM pins shorted internally
V1.8_DDR_CAP1
V1.8_DDR_CAP2
V1.8_DDR_CAP5
V1.8_DDR_CAP6
V1.8_DDR_CAP4
V1.8_DDR_CAP3
U38E
71.0GMCH.08U
POWER
Route ASSATVBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane
Route ASSA3GBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane
VCC 1D05_S0 for low speed graphic clock.1D5V_S0 for high speed clock.default use 1D05V_S0
AG1-910-SB
R178
0R0805-PAD
L5
L3
L13
L12
C141
C150
C136
C135
C226
C334
C225
C333
1D5V_HMPLL_S0
1D5V_DPLLA_S0
1D5V_DPLLB_S0
1D5V_HPLL_S0
1D5V_MPLL_S0
R276
0R3-0-U-GP
R277
0R0603-PAD
C318
SC4D7U6D3V3KX-GP
C314
R163
0R0402-PAD
C319
R278
1KR2J-1-GP
D27
SSM5818SLPT-GP
DY
C324
SCD47U10V3ZY-GP
C325
C328
C329
SCD22U16V2ZY-GP
C185
SC4D7U10V5ZY-3GP
C210
C184
SCD1U16V2ZY-2GP
SC2D2U6D3V3MX-1-GP
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
<Core Design>
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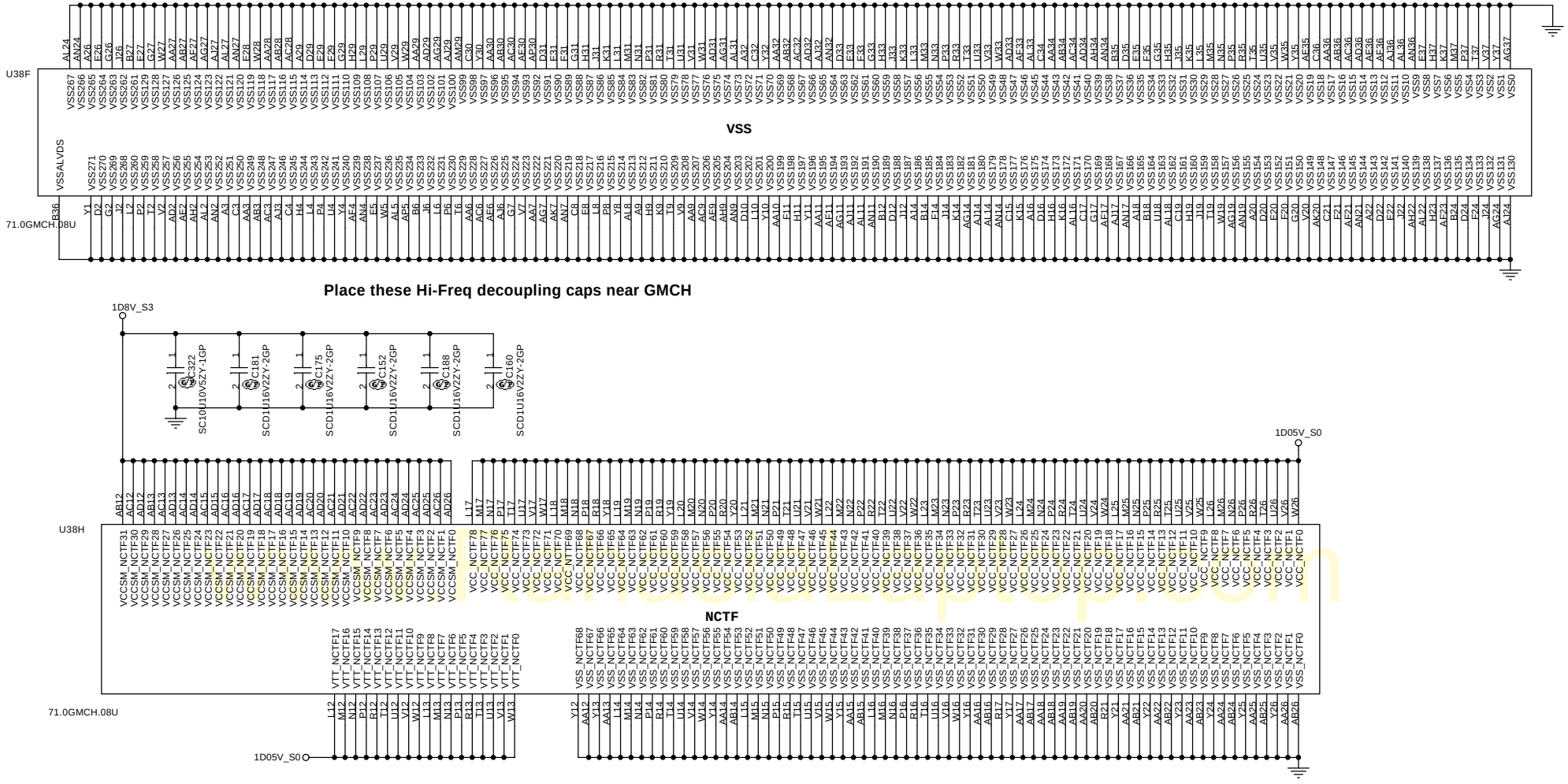
Title
GMCH (4 of 5)
Size A3
Document Number
AG1(Alviso)
Rev 01
Date: Monday, October 17, 2005
Sheet 9 of 40



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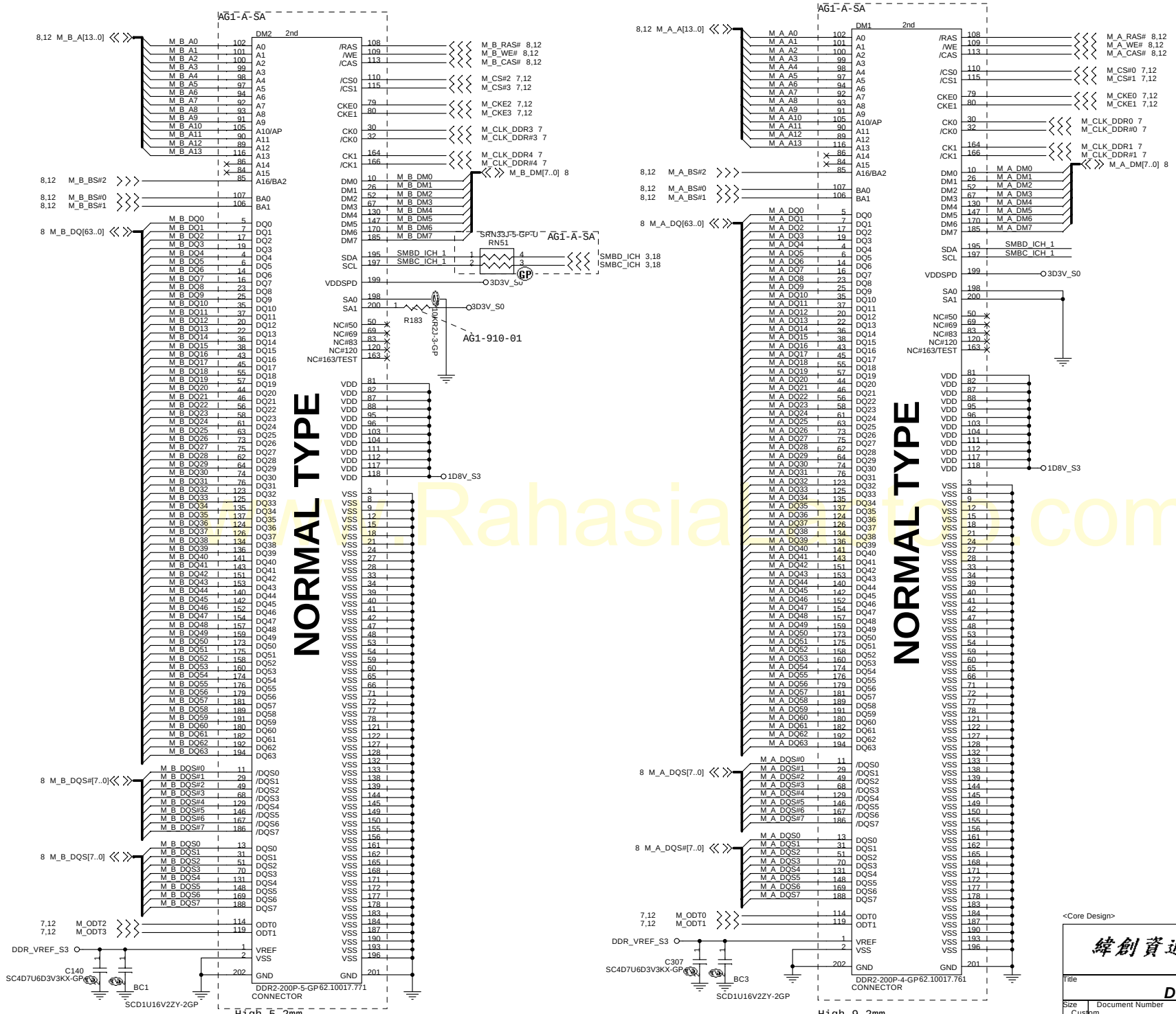
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GMCH (5 of 5)***	
Size A3	Document Number **AG1(Alviso)**	Rev **01**
Date: Monday, October 17, 2005	Sheet 10 of 40	



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Title: ***DDR Socket***

Size: Custom | Document Number: **AG1(Alviso)** | Rev: **01**

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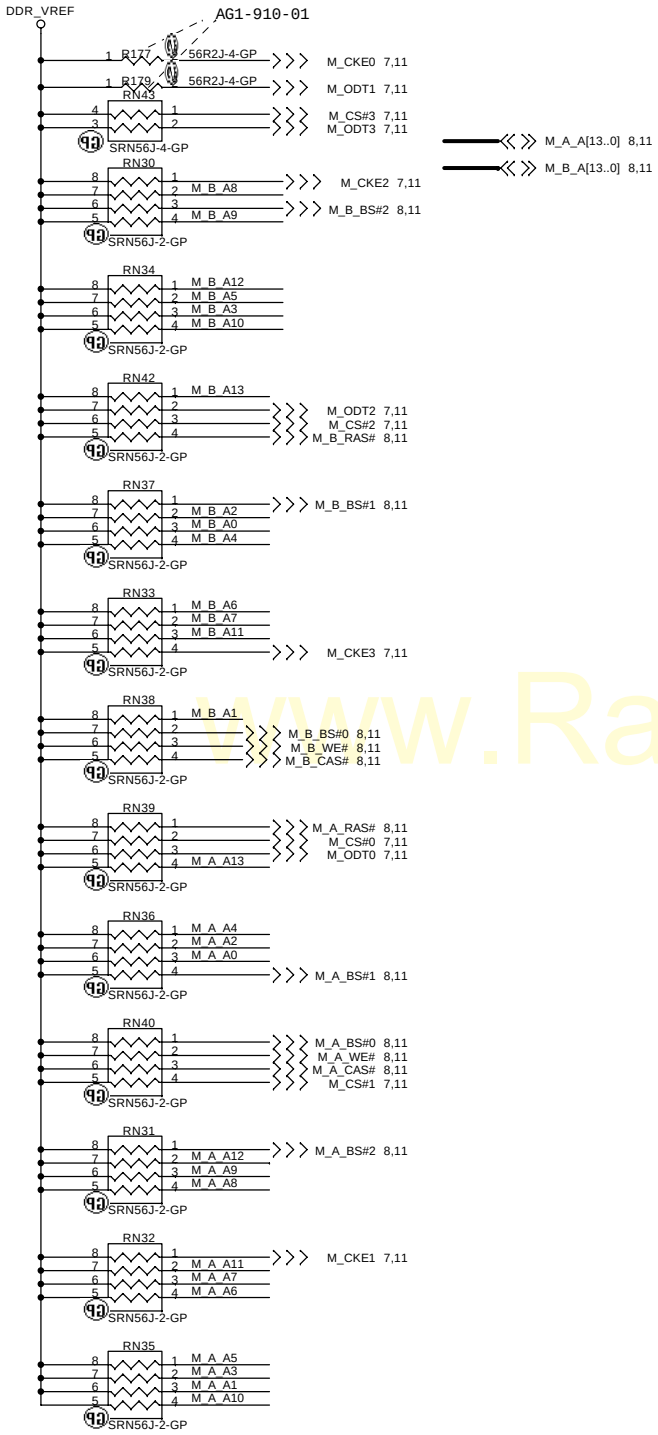
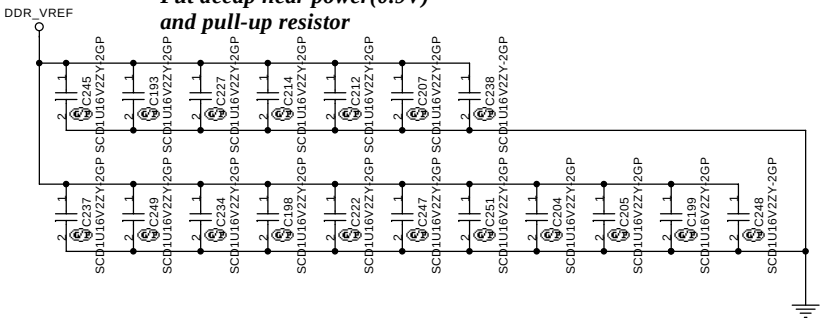
PARALLEL TERMINATION

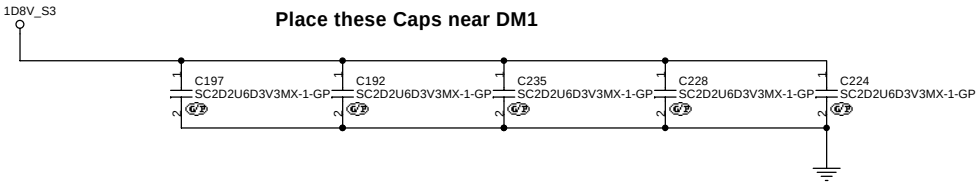
Put decap near power(0.9V) and pull-up resistor

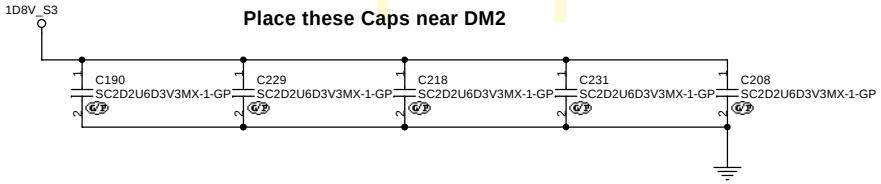


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor







<Core Design>

緯創資通 **Wistron Corporation**
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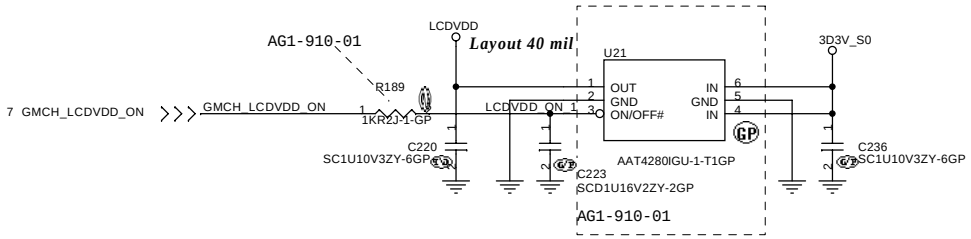
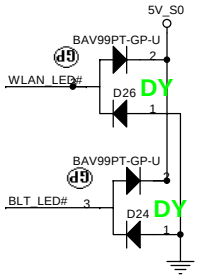
Title: ***DDR2 Termination Resistor***

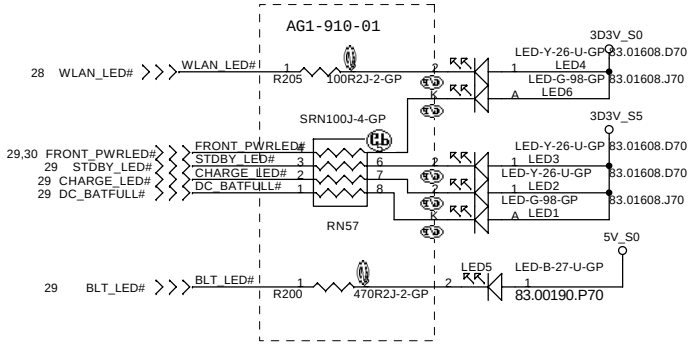
Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Tuesday, October 25, 2005 | Sheet 12 of 40

LED







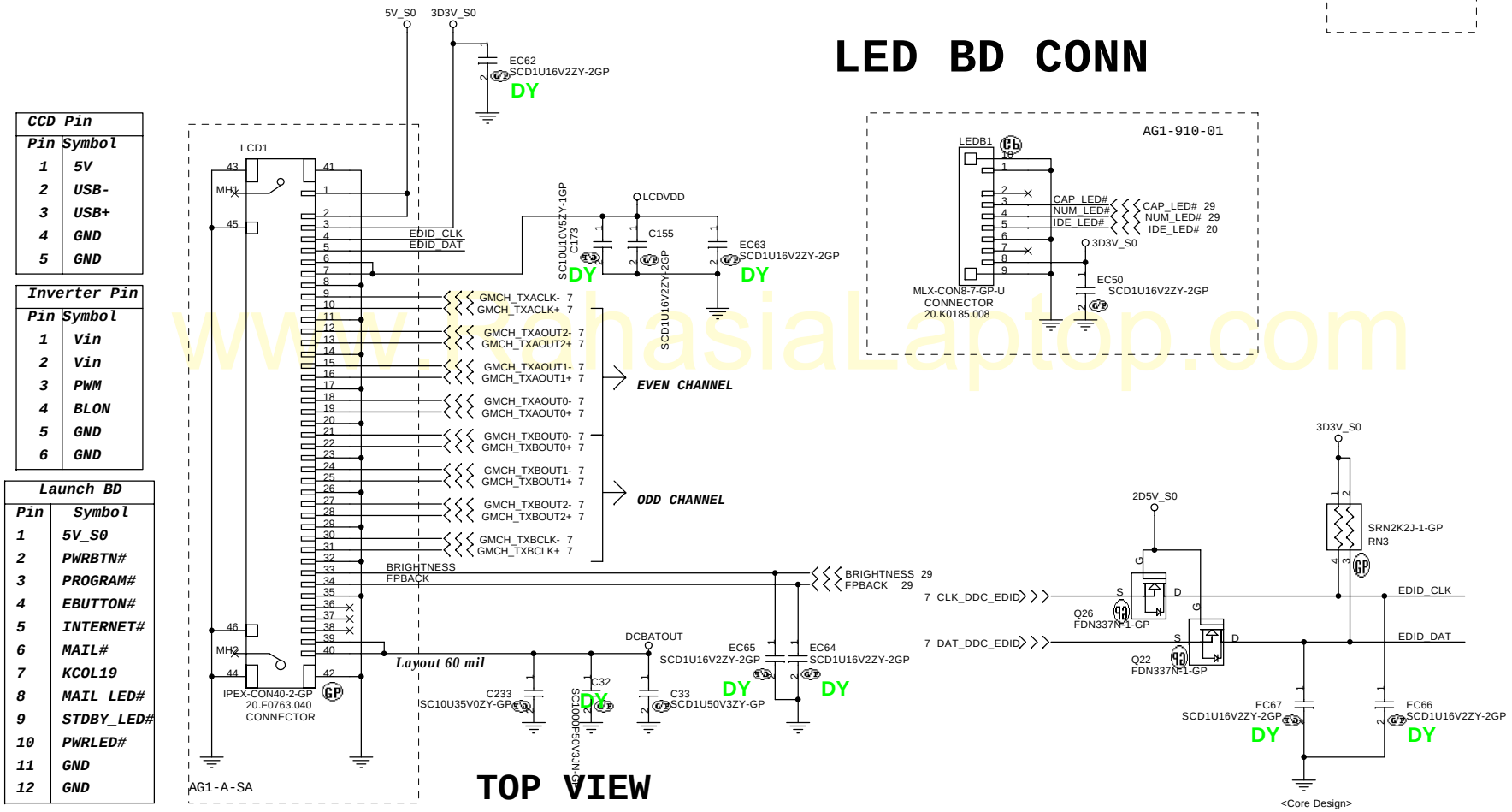
LCD/INVERTER/CCD CONN

LED BD CONN

CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	5V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	KCOL19
8	MAIL_LED#
9	STDBY_LED#
10	PWRLED#
11	GND
12	GND

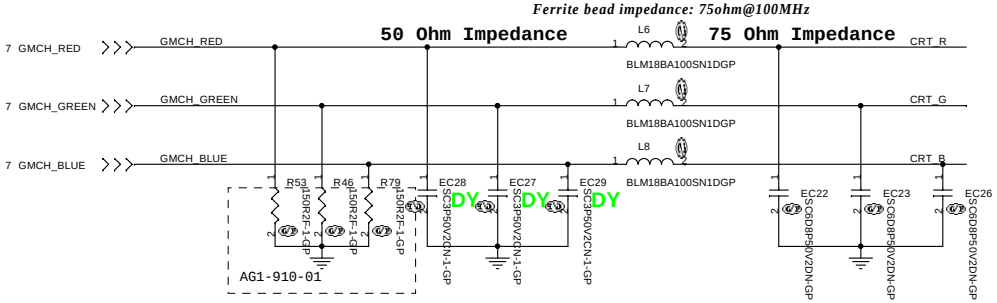


TOP VIEW

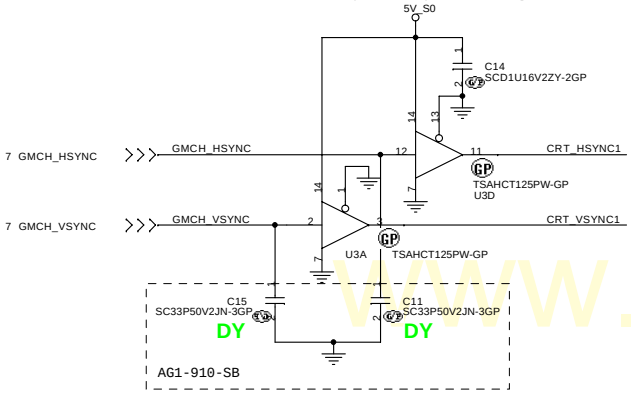
LCD

CRT CONNECTOR

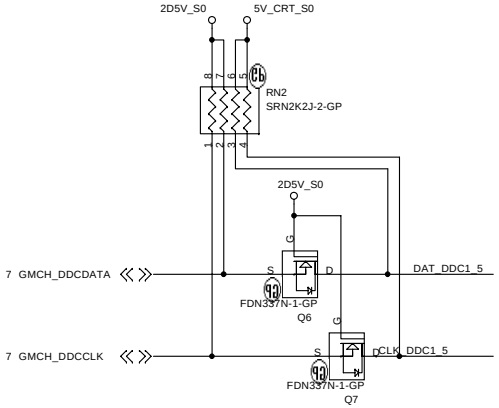
Ferrite bead impedance: 75ohm@100MHz

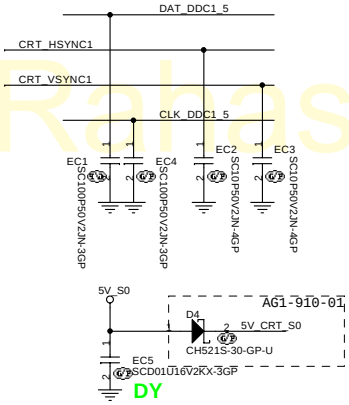


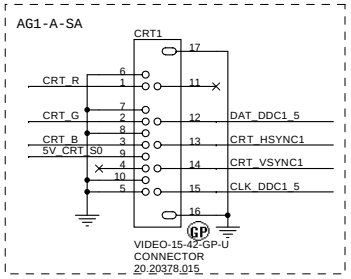
Hsync & Vsync level shift



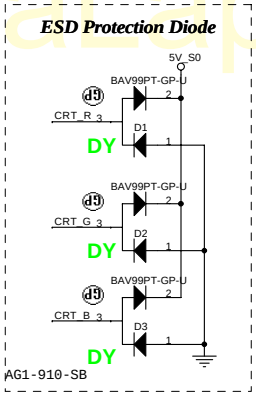
DDC_CLK & DATA level shift







ESD Protection Diode



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT Connector*

Size: Custom | Document Number: AG1(Alviso) | Rev: 01

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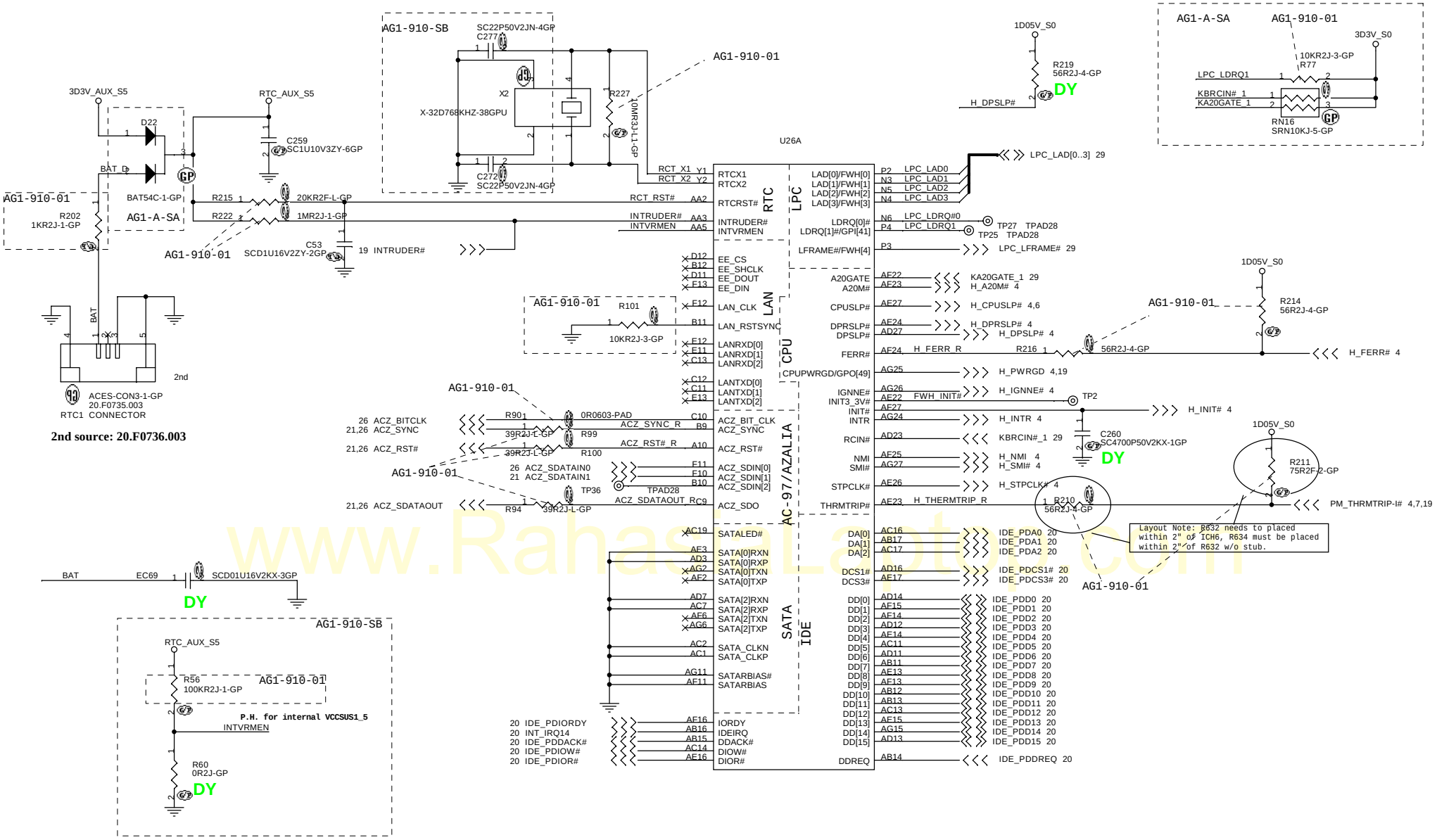
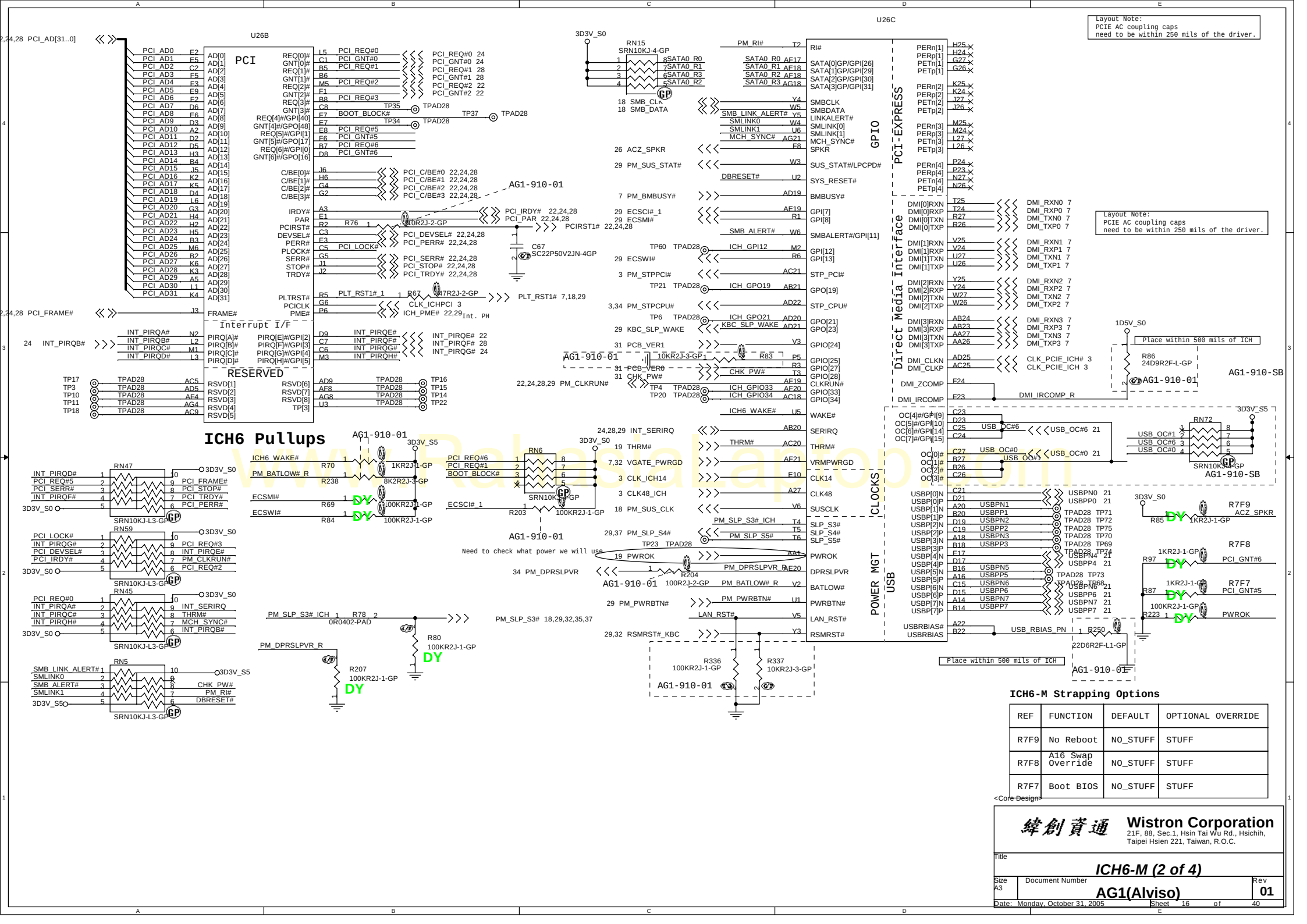


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*ICH6-M (1 of 4)*
Size A3	Document Number **AG1(Alviso)** Rev **01**
Date: Thursday, October 27, 2005	Sheet 15 of 40



ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH6-M (2 of 4)*

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

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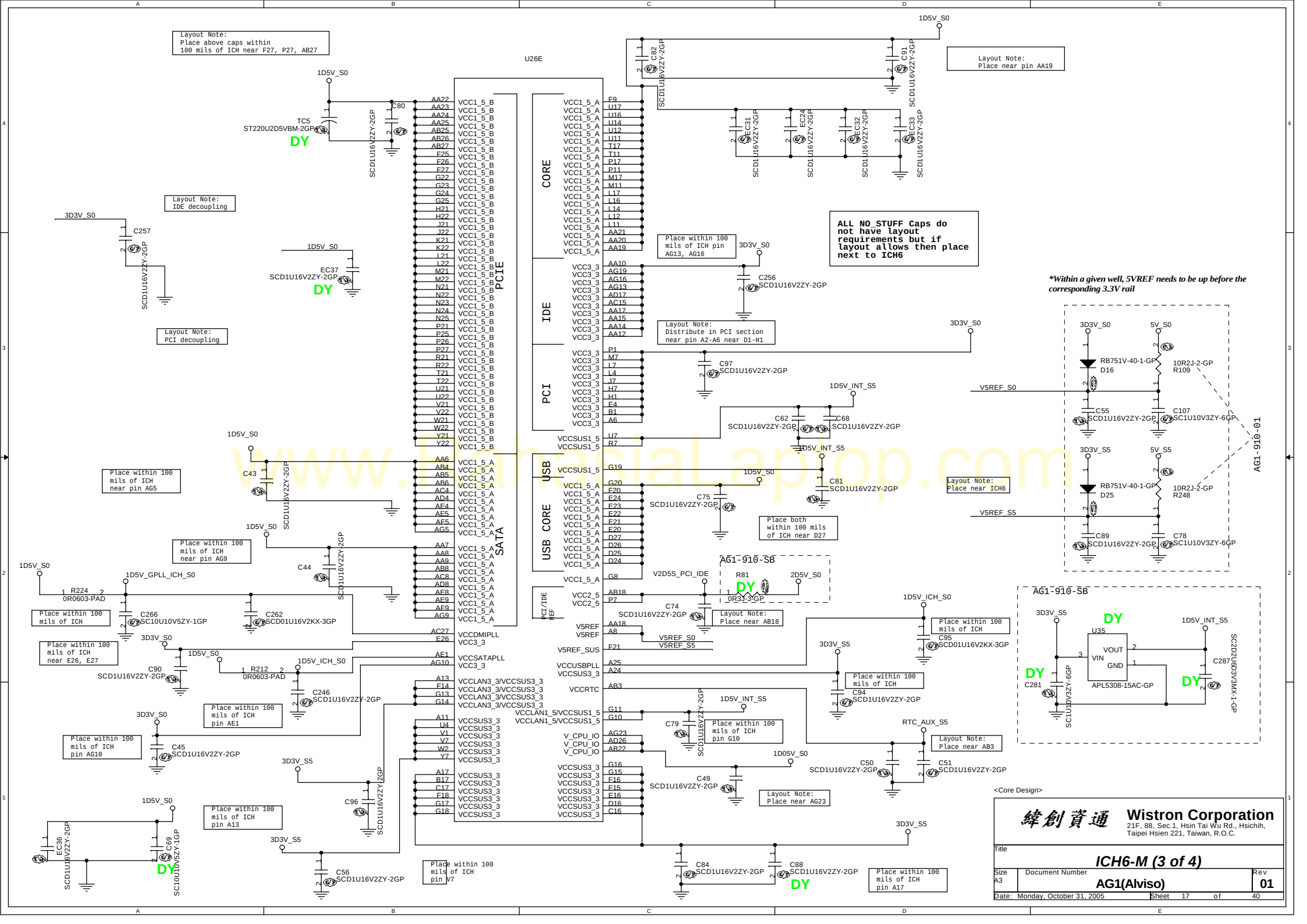
Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27
U26E
1D5V_S0
C80
SCD1U16V2ZY-2GP
TC5
ST220U2D5VBM-2GP
DY
Layout Note:
IDE decoupling
3D3V_S0
C257
SCD1U16V2ZY-2GP
EC37
Layout Note:
PCI decoupling
Place within 100
mils of ICH
near pin AG5
C43
Place within 100
mils of ICH
near pin AG9
C44
Place within 100
mils of ICH
near E26, E27
C90
R212
0R0603-PAD
C246
Place within 100
mils of ICH
pin AE1
Place within 100
mils of ICH
pin AG10
C45
Place within 100
mils of ICH
pin A13
C96
C56
SCD1U16V2ZY-2GP
Place within 100
mils of ICH
pin V7
C84
C88
Place within 100
mils of ICH
pin A17
EC36
C69
SC10U10V5ZY-1GP
R224
0R0603-PAD
C266
SC10U10V5ZY-1GP
C262
SCD01U16V2KX-3GP
1D5V_GPLL_ICH_S0
1D5V_ICH_S0
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
VCC1_5_B
VCC1_5_A
VCC3_3
VCCSUS1_5
VCCSUS3_3
VCCLAN3_3/VCCSUS3_3
VCCLAN1_5/VCCSUS1_5
VCCDMIPLL
VCCSATAPLL
V5REF
V5REF_SUS
VCCUSBPLL
VCCRTC
V_CPU_IO
C82
C91
SCD1U16V2ZY-2GP
Layout Note:
Place near pin AA19
EC31
EC24
EC32
EC33
ALL NO_STUFF Caps do
not have layout
requirements but if
layout allows then place
next to ICH6
Place within 100
mils of ICH pin
AG13, AG16
C256
Layout Note:
Distribute in PCI section
near pin A2-A6 near D1-H1
C97
1D5V_INT_S5
C62
C68
SCD1U16V2ZY-2GP
C75
C81
Place both
within 100 mils
of ICH near D27
AG1-910-SB
V2D5S_PCI_IDE
R81
0R3J-3-GP
2D5V_S0
C74
Layout Note:
Place near AB18
V5REF_S0
V5REF_S5
Layout Note:
Place near AG23
C79
Place within 100
mils of ICH
pin G10
C49
C50
C51
RTC_AUX_S5
Layout Note:
Place near AB3
1D05V_S0
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
5V_S0
RB751V-40-1-GP
D16
10R2J-2-GP
R109
C55
C107
SC1U10V3ZY-6GP
V5REF_S0
D25
R248
C89
C78
V5REF_S5
AG1-910-01
Layout Note:
Place near ICH6
Place within 100
mils of ICH
C95
SCD01U16V2KX-3GP
C94
SCD1U16V2ZY-2GP
U35
VOUT
VIN
GND
APL5308-15AC-GP
C281
C287
SC2D2U6D3V3MX-1-GP
SC1U10V3ZY-6GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size
A3
Document Number
AG1(Alviso)
Rev
01
Date: Monday, October 31, 2005
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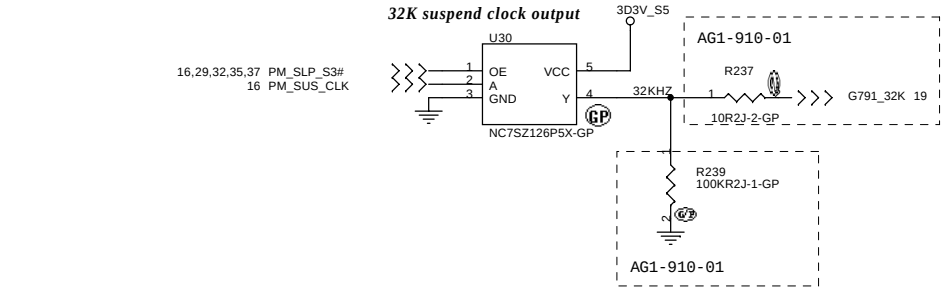

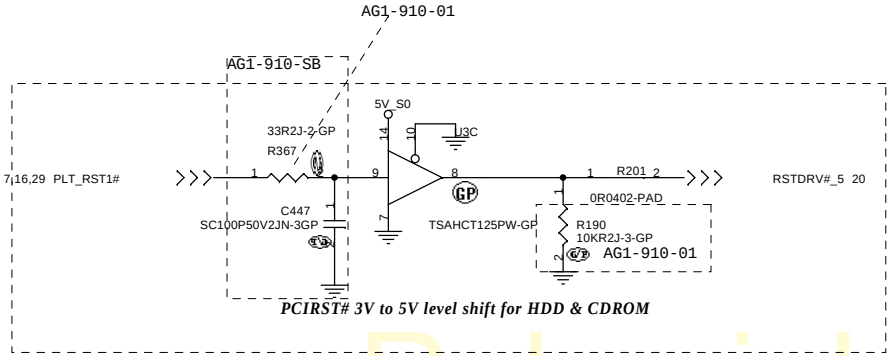

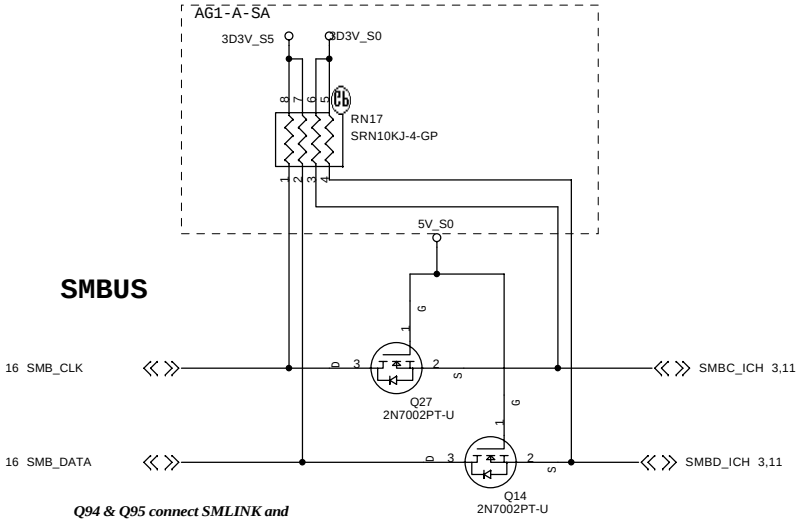

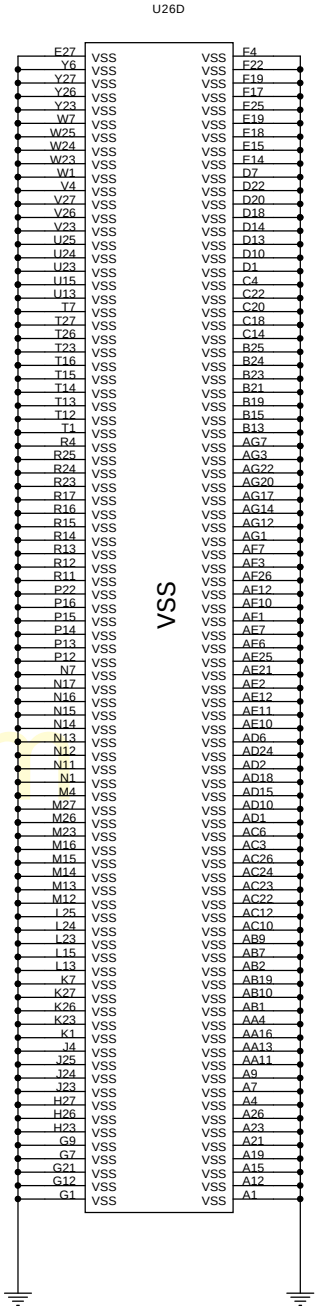

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ICH6-M (4 of 4)***

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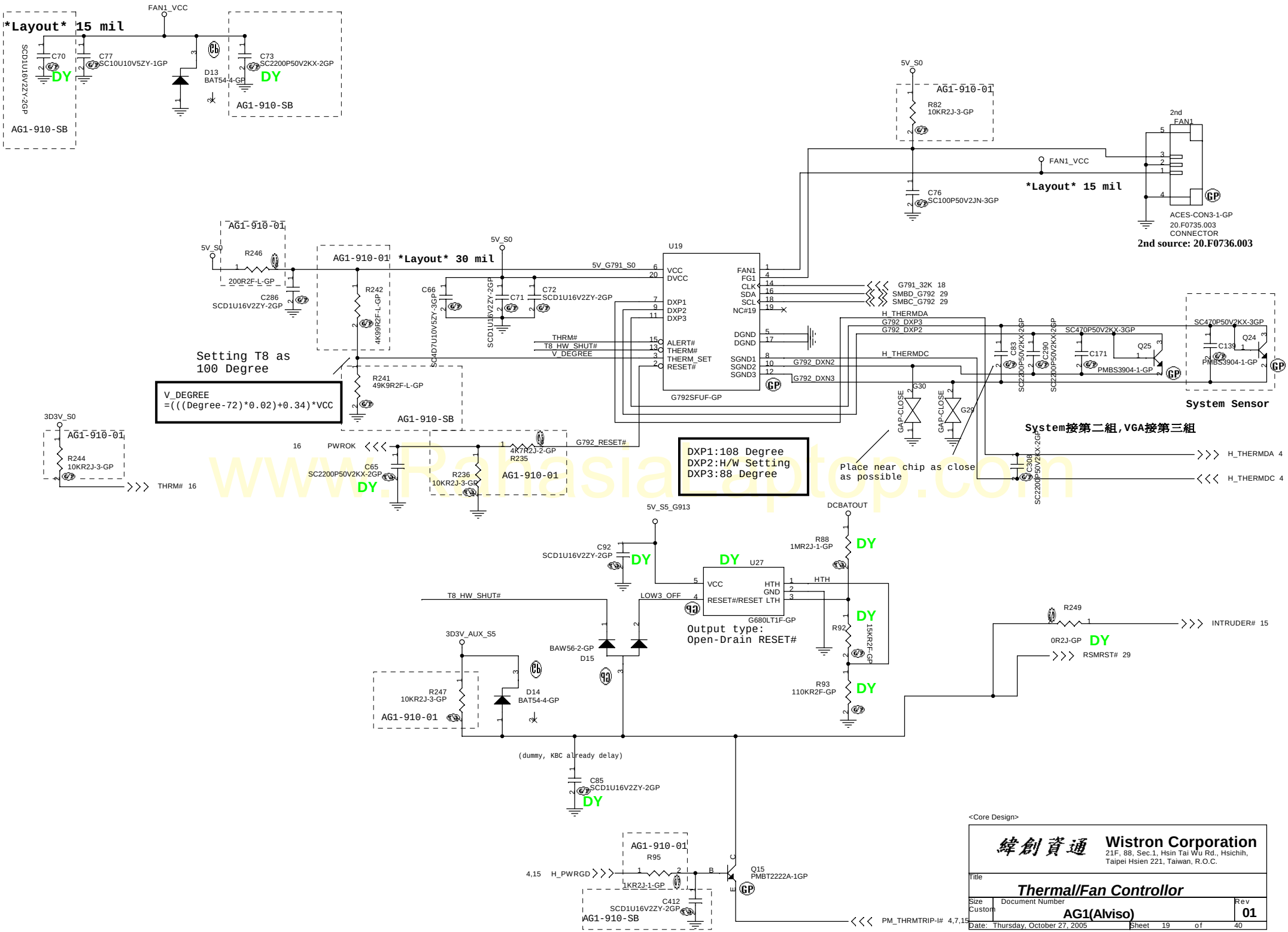
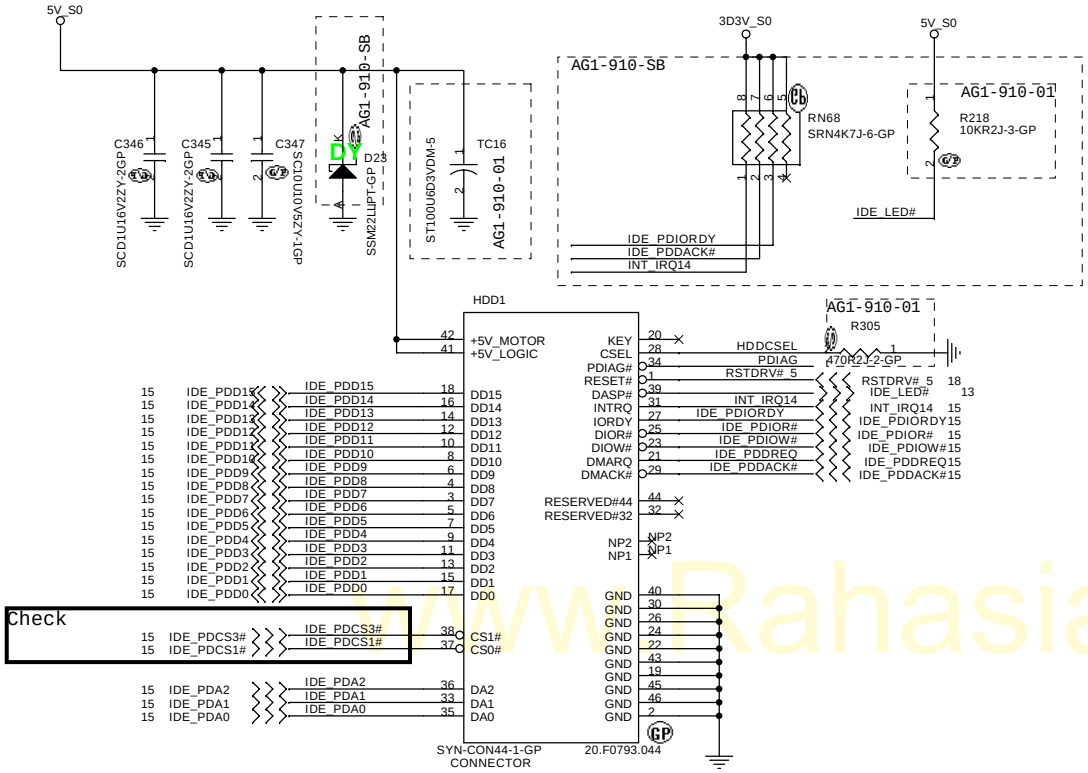
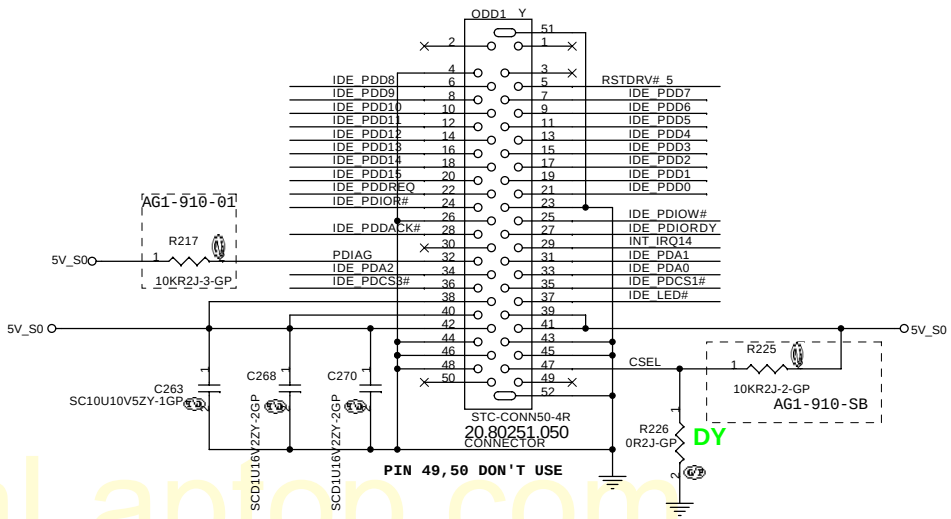


HDD Connector



CD-ROM Connector



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***HDD and CDROM***
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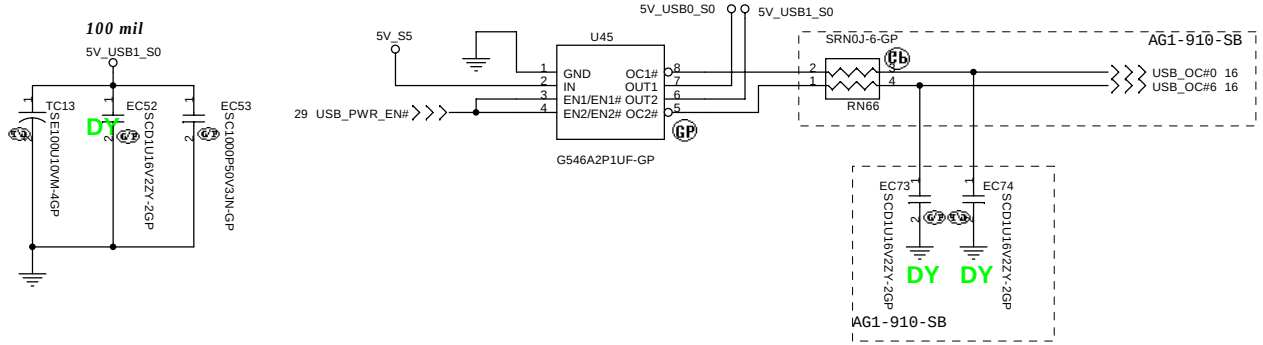
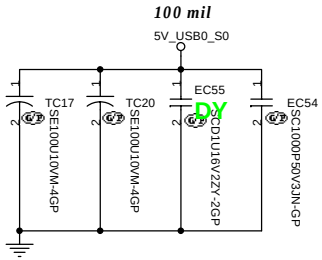
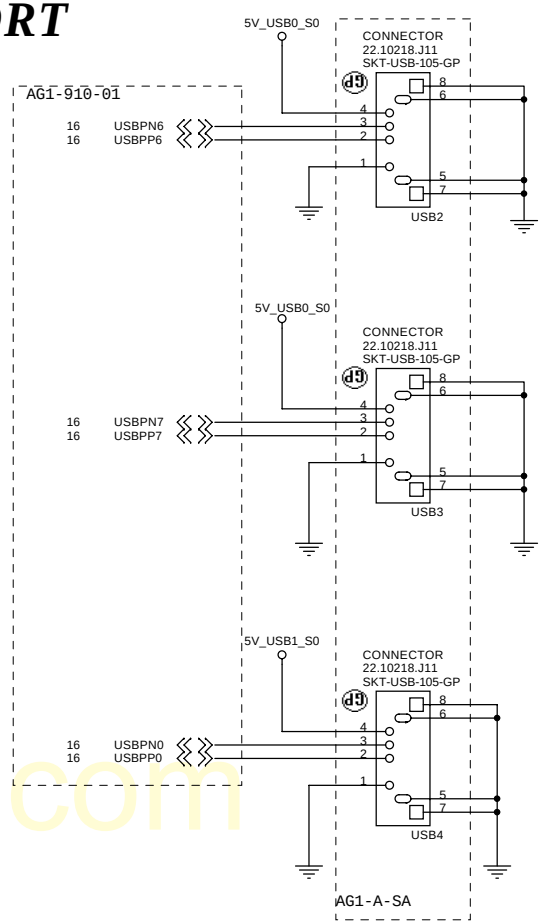
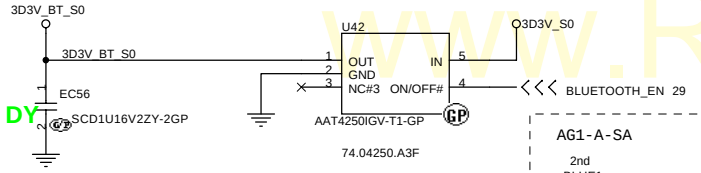
USB PORT

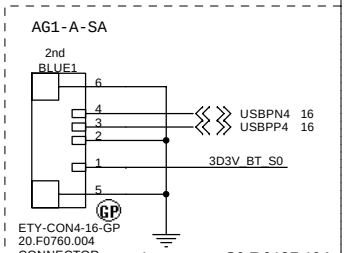






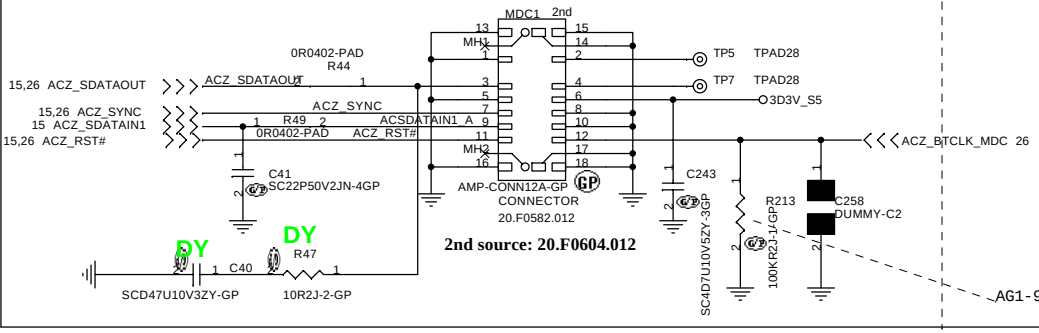
BLUETOOTH MODULE





1st source: 20.D0197.104

MDC 1.5 CONNECTOR



2nd source: 20.F0604.012

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**USB / MDC / BLUETOOTH**
Size A3	Document Number: **AG1(Alviso)** — Rev: **01**
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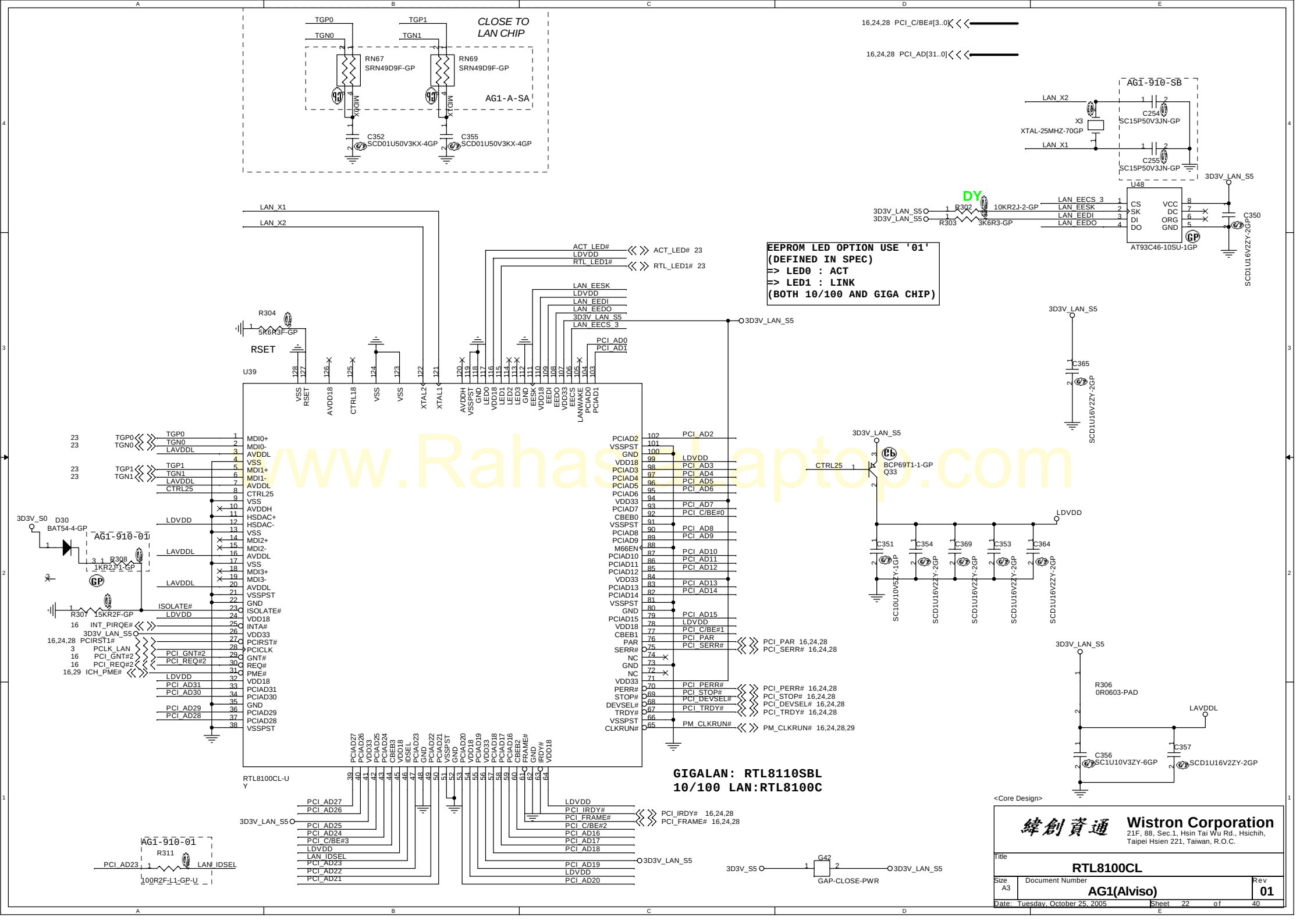
CLOSE TO LAN CHIP
RN67 SRN49D9F-GP
RN69 SRN49D9F-GP
AG1-A-SA
C352 SCD01U50V3KX-4GP
C355 SCD01U50V3KX-4GP
16,24,28 PCI_C/BE#[3..0]
16,24,28 PCI_AD[31..0]
AG1-910-SB
X3 XTAL-25MHZ-70GP
C254 SC15P50V3JN-GP
C255 SC15P50V3JN-GP
DY
R302 10KR2J-2-GP
R303 3K6R3-GP
U48
AT93C46-10SU-1GP
C350 SCD1U16V2ZY-2GP
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
R304 5K6R3F-GP
RSET
U39
C365 SCD1U16V2ZY-2GP
Q33 BCP69T1-1-GP
C351 SC10U10V5ZY-1GP
C354 SCD1U16V2ZY-2GP
C369 SCD1U16V2ZY-2GP
C353 SCD1U16V2ZY-2GP
C364 SCD1U16V2ZY-2GP
D30 BAT54-4-GP
AG1-910-01
R308 1KR2J-1-GP
R307 15KR2F-GP
R306 0R0603-PAD
C356 SC1U10V3ZY-6GP
C357 SCD1U16V2ZY-2GP
RTL8100CL-UY
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
AG1-910-01
R311 100R2F-L1-GP-U
G42 GAP-CLOSE-PWR
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8100CL
Size A3
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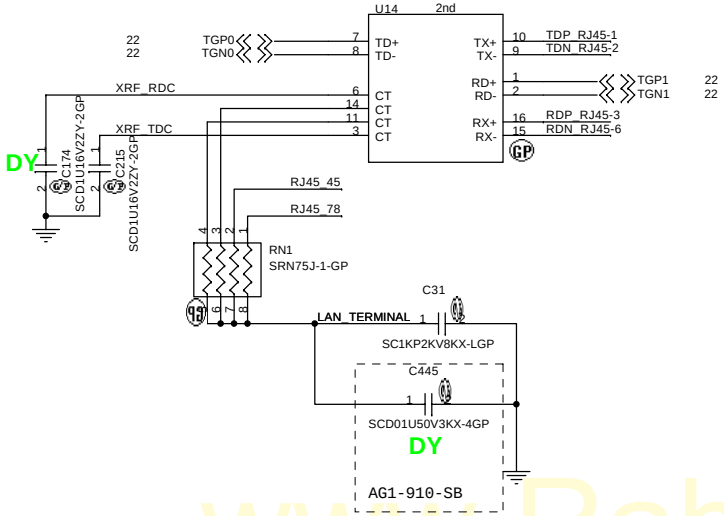
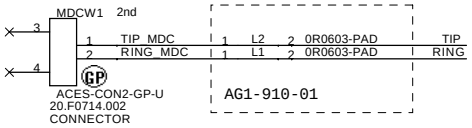
10/100M Lan Transformer

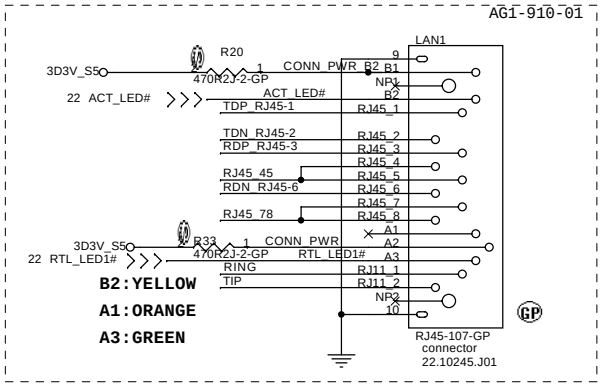


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



2nd source: 20.D0196.102

LAN Connector



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN CONN		
Size: A3	Document Number: AG1(Alviso)	Rev: 01
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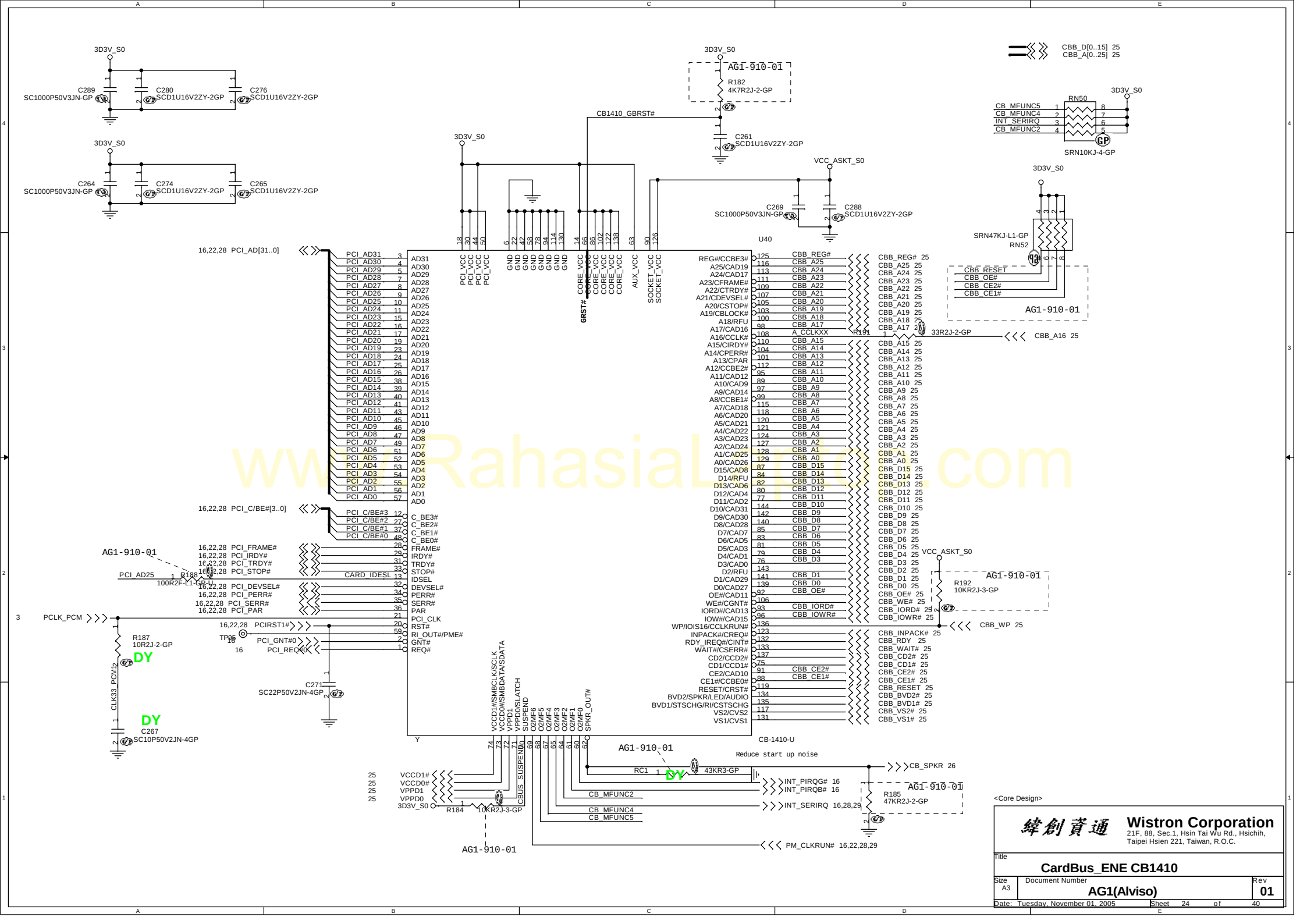
3D3V_S0
C289 SC1000P50V3JN-GP
C280 SCD1U16V2ZY-2GP
C276 SCD1U16V2ZY-2GP
C264 SC1000P50V3JN-GP
C274 SCD1U16V2ZY-2GP
C265 SCD1U16V2ZY-2GP
AG1-910-01
R182 4K7R2J-2-GP
CB1410_GBRST#
C261 SCD1U16V2ZY-2GP
VCC_ASKT_S0
C269 SC1000P50V3JN-GP
C288 SCD1U16V2ZY-2GP
CBB_D[0..15] 25
CBB_A[0..25] 25
RN50
CB_MFUNC5
CB_MFUNC4
INT_SERIRQ
CB_MFUNC2
SRN10KJ-4-GP
SRN47KJ-L1-GP
RN52
CBB_RESET
CBB_OE#
CBB_CE2#
CBB_CE1#
16,22,28 PCI_AD[31..0]
16,22,28 PCI_C/BE#[3..0]
16,22,28 PCI_FRAME#
16,22,28 PCI_IRDY#
16,22,28 PCI_TRDY#
16,22,28 PCI_STOP#
16,22,28 PCI_DEVSEL#
16,22,28 PCI_PERR#
16,22,28 PCI_SERR#
16,22,28 PCI_PAR
16,22,28 PCIRST1#
PCI_GNT#0
PCI_REQ#0
CARD_IDESL
PCI_AD25
R188 100R2F-L1-GP-U
PCLK_PCM
R187 10R2J-2-GP
DY
CLK33_PCM
C267 SC10P50V2JN-4GP
C271 SC22P50V2JN-4GP
U40
CB-1410-U
GRST#
CBB_REG#
CBB_A16 25
R191 33R2J-2-GP
R192 10KR2J-3-GP
CBB_WP 25
CBB_IORD# 25
CBB_IOWR# 25
CBB_INPACK# 25
CBB_RDY 25
CBB_WAIT# 25
CBB_CD2# 25
CBB_CD1# 25
CBB_CE2# 25
CBB_CE1# 25
CBB_RESET 25
CBB_BVD2# 25
CBB_BVD1# 25
CBB_VS2# 25
CBB_VS1# 25
Reduce start up noise
RC1 43KR3-GP
CB_SPKR 26
INT_PIRQG# 16
INT_PIRQB# 16
R185 47KR2J-2-GP
INT_SERIRQ 16,28,29
R184 10KR2J-3-GP
CBUS_SUSPEND
CB_MFUNC2
CB_MFUNC4
CB_MFUNC5
PM_CLKRUN# 16,22,28,29
VCCD1#
VCCD0#
VPPD1
VPPD0
3D3V_S0
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CardBus_ENE CB1410
Size A3
Document Number AG1(Alviso)
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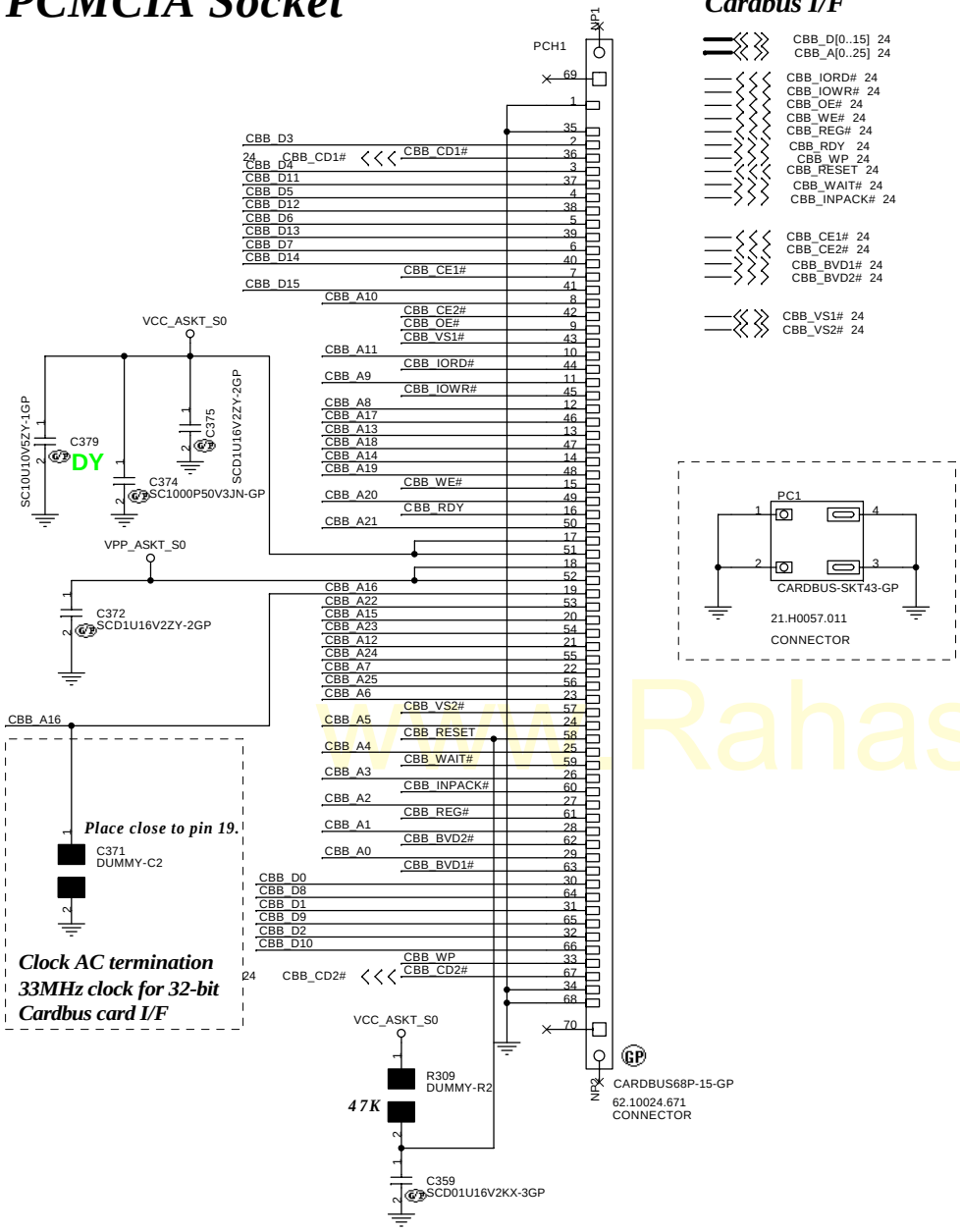
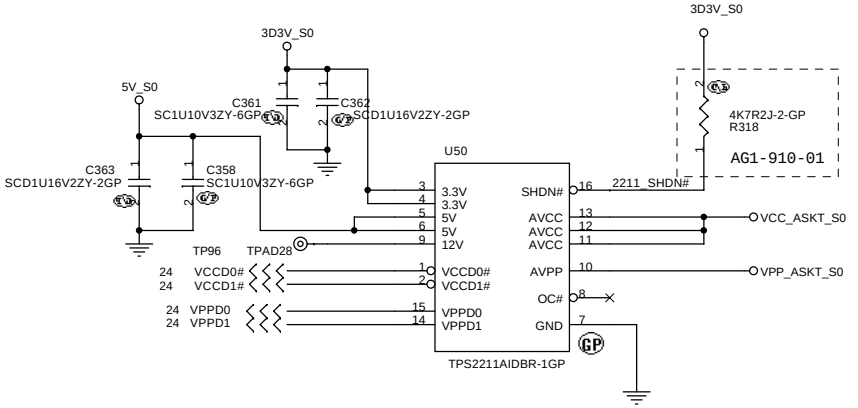
PCMCIA Socket



Cardbus I/F

Power switch



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: PCMCA	
Size: A3	Document Number: AG1(Alviso)
Rev: 01	
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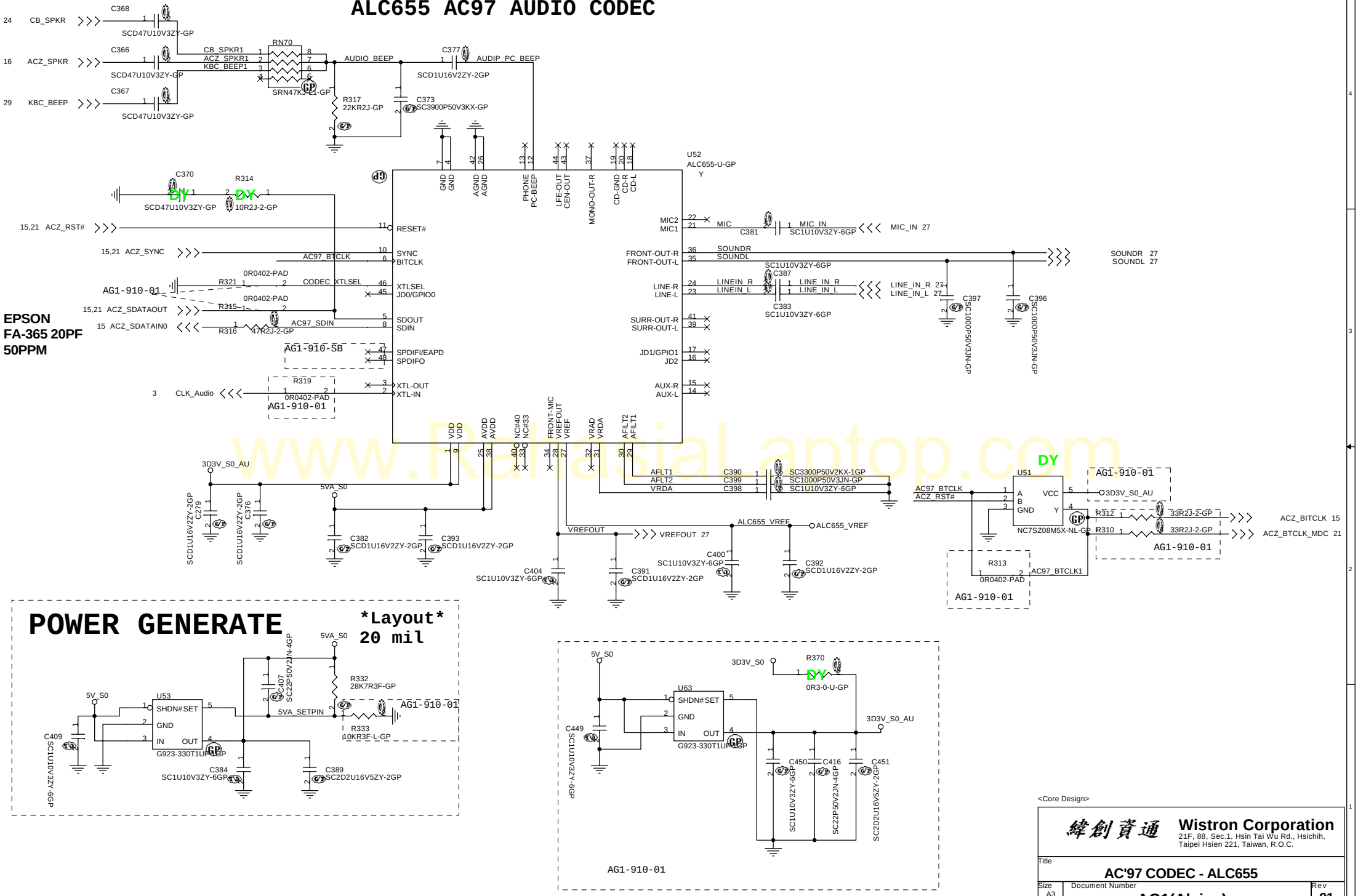
ALC655 AC97 AUDIO CODEC

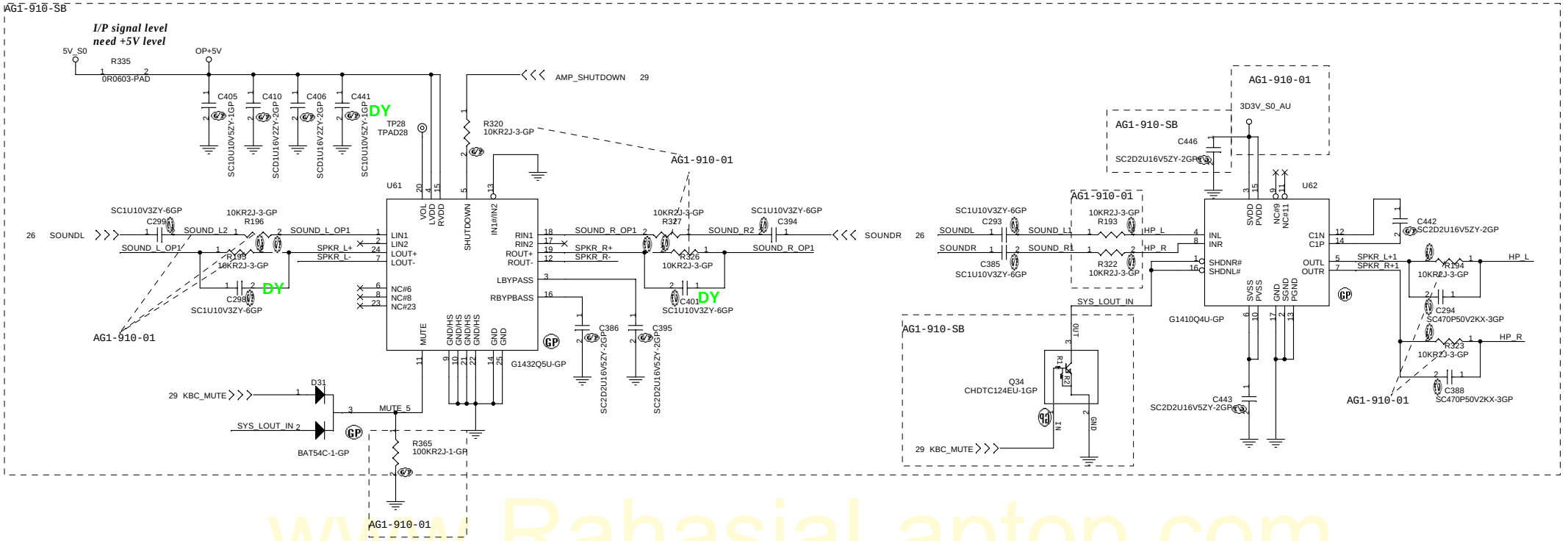


<Core Design>

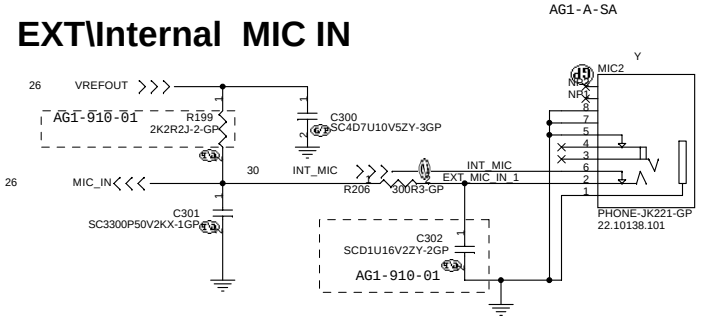
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AC'97 CODEC - ALC655	
Size A3	Document Number AG1(Alviso)	Rev 01
Date: Tuesday, November 01, 2005	Sheet 26 of 40	

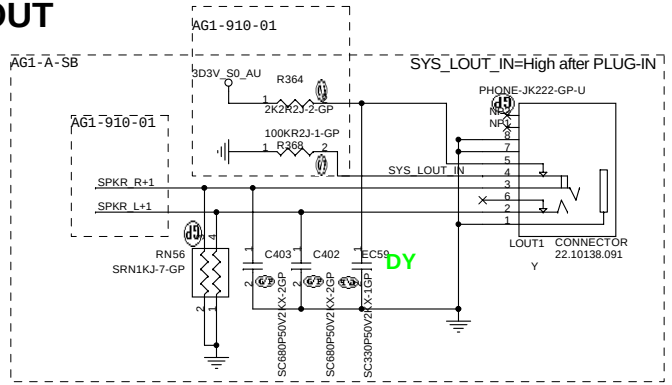
AUDIO OP AMPLIFIER



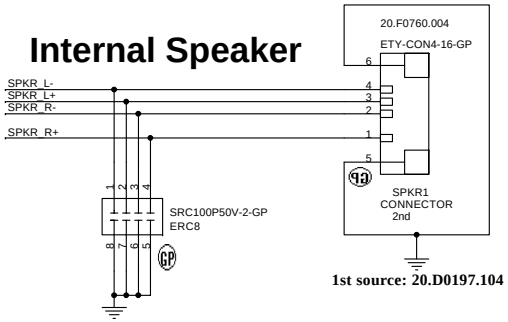
EXT\Internal MIC IN



LINE OUT



Internal Speaker



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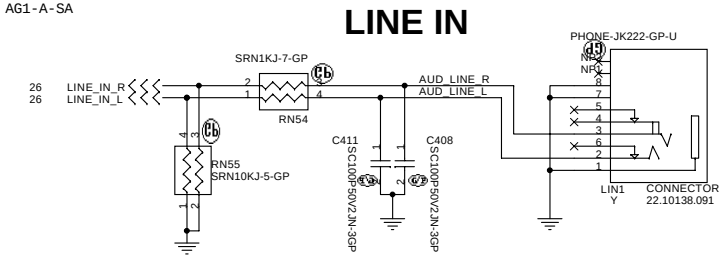

<Core Design>

Wistron Corporation
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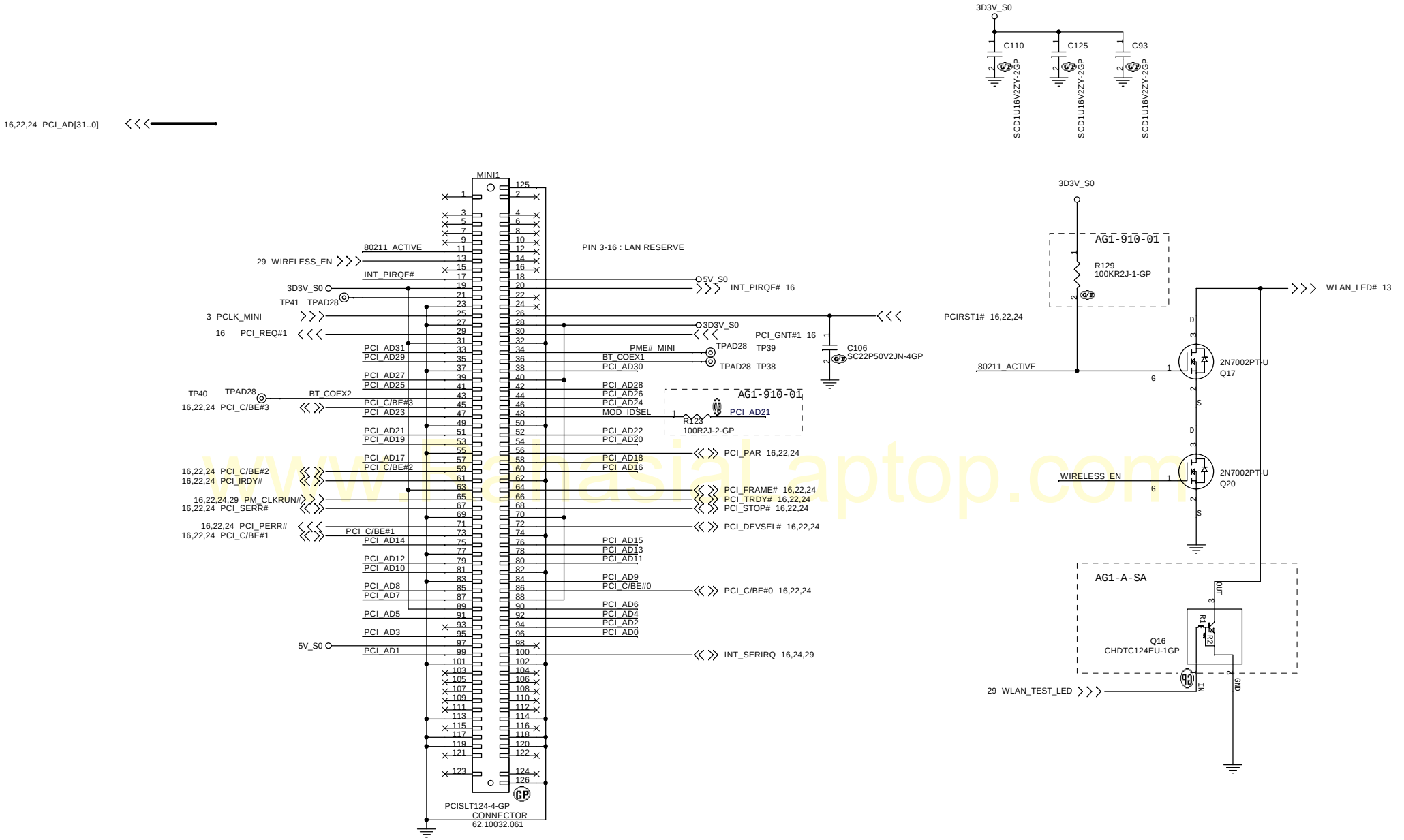
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio AMP and Jack	
Size	Document Number	Rev
	AG1(Alviso)	01
Date: Monday, October 31, 2005	Sheet 27 of 40	



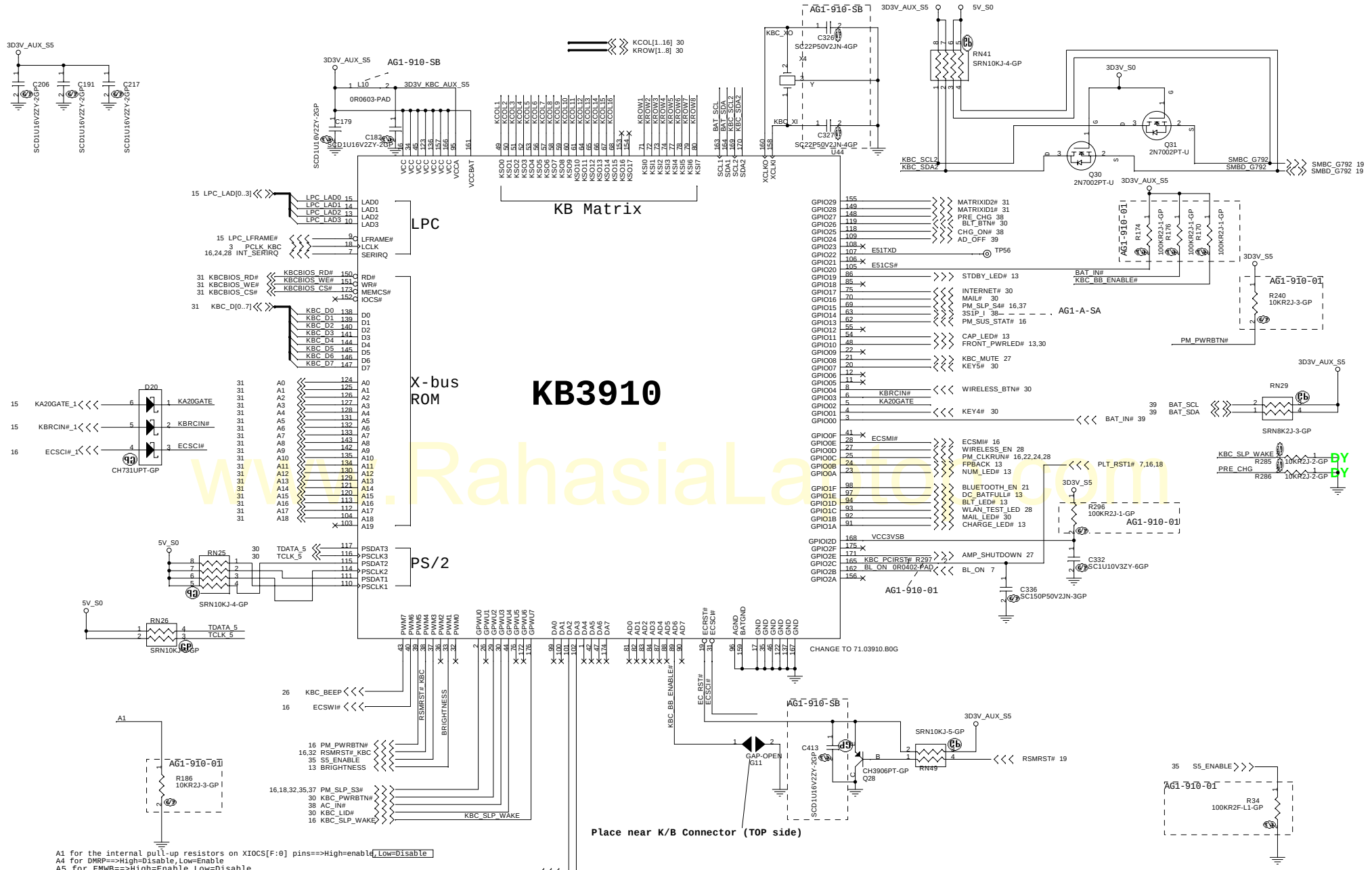
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

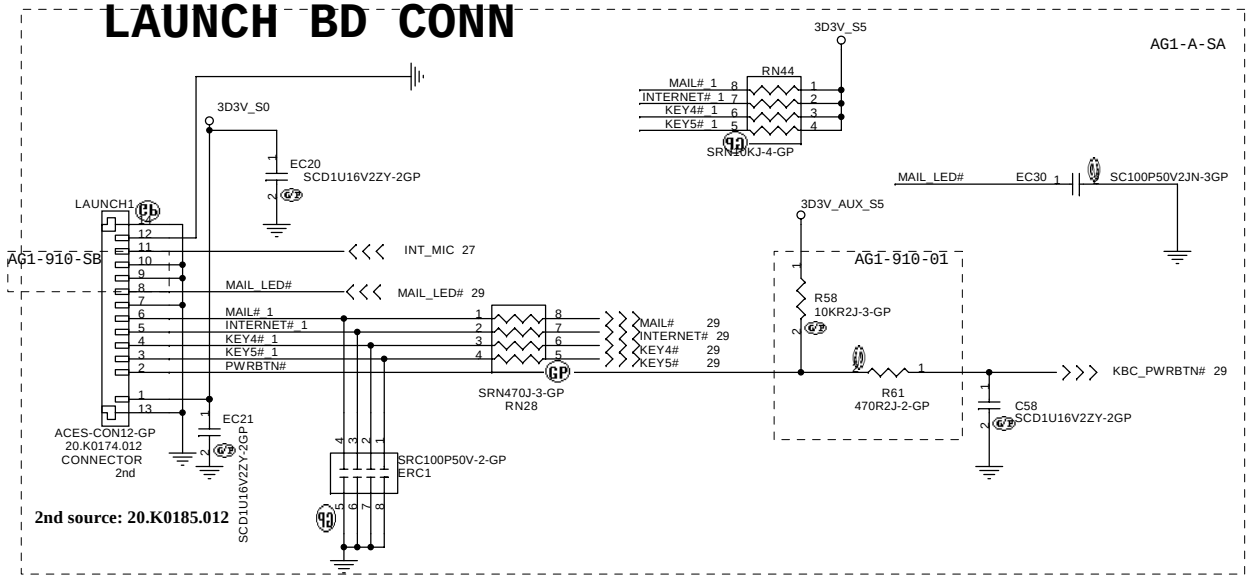
Title: ***MINI-PCI***

Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

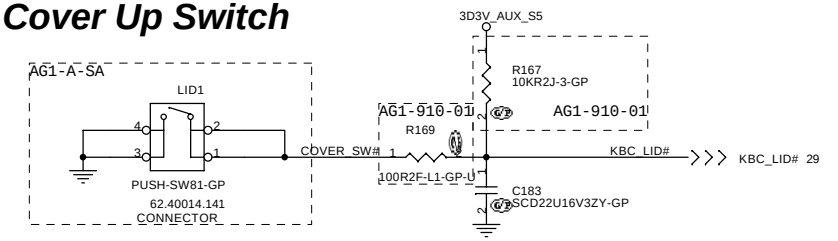
Date: Tuesday, October 25, 2005 | Sheet 28 of 40



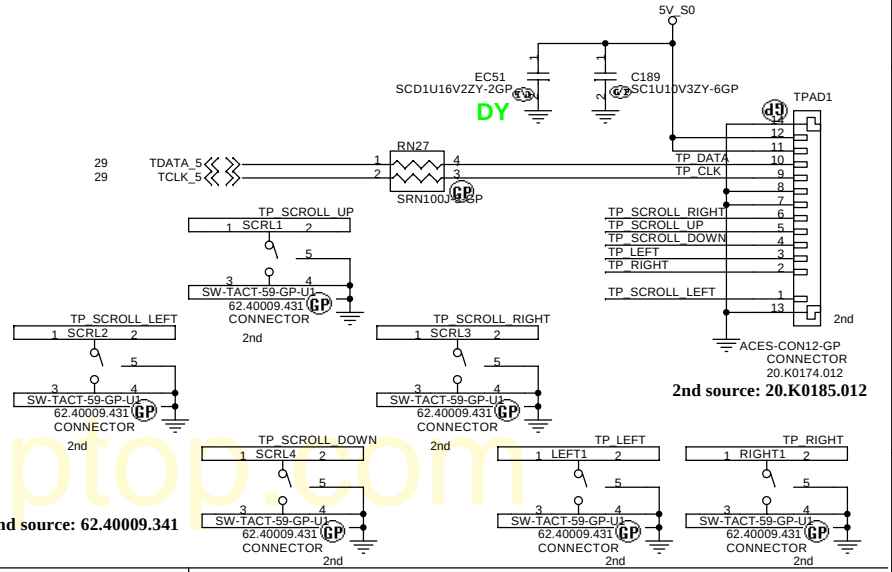
LAUNCH BD CONN

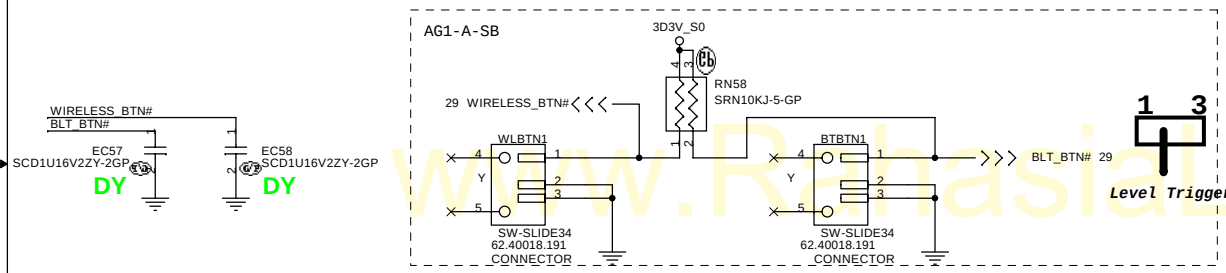


Cover Up Switch

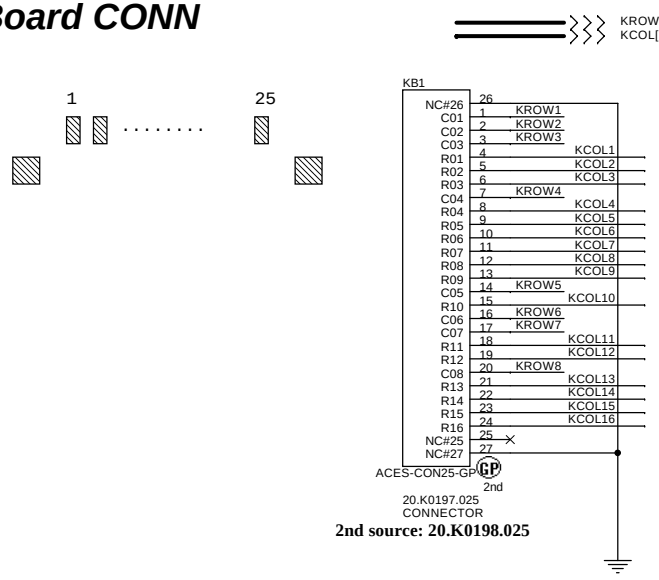


TOUCH PAD



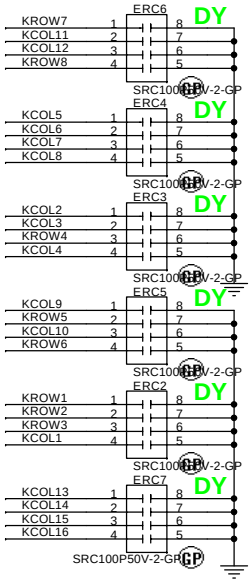


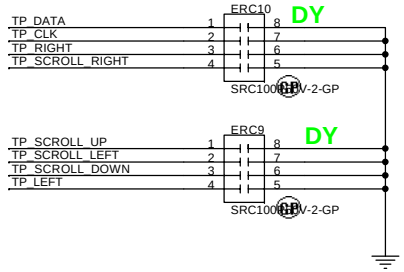
Internal KeyBoard CONN



Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.





<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONs / KB / TOUCHPAD**

Size	Document Number	Rev
A3	AG1-910	01

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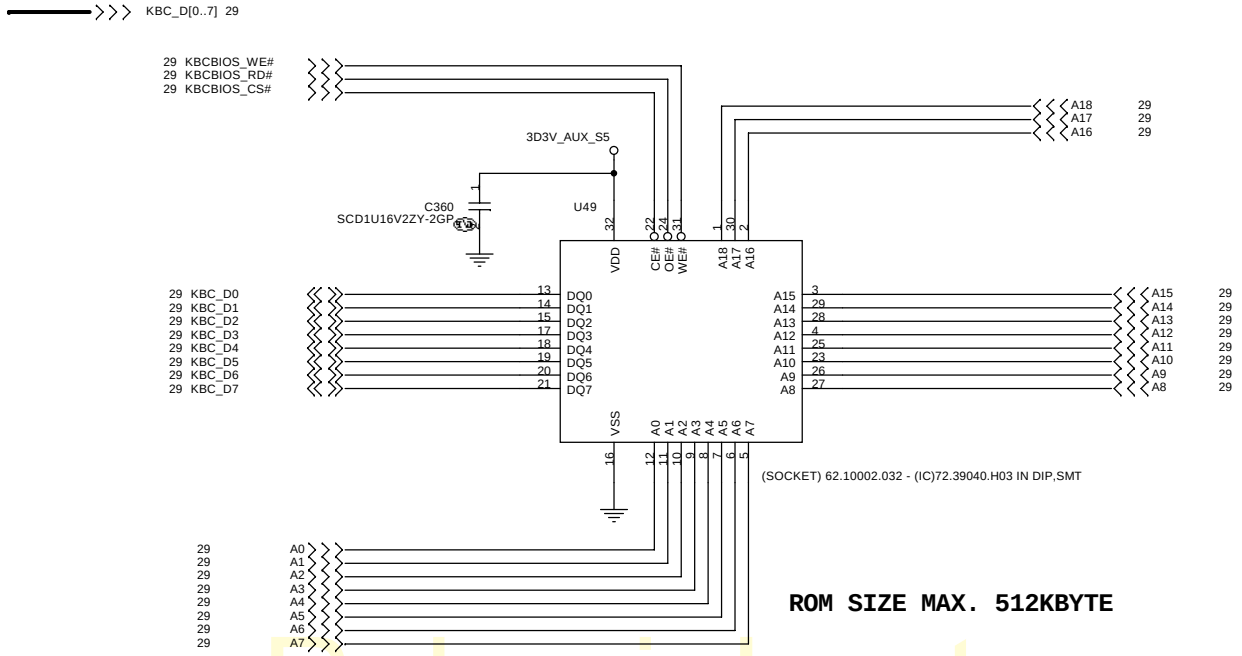
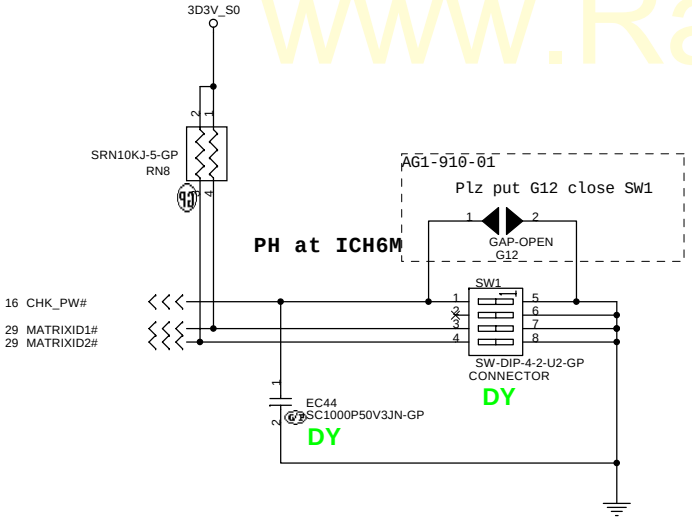


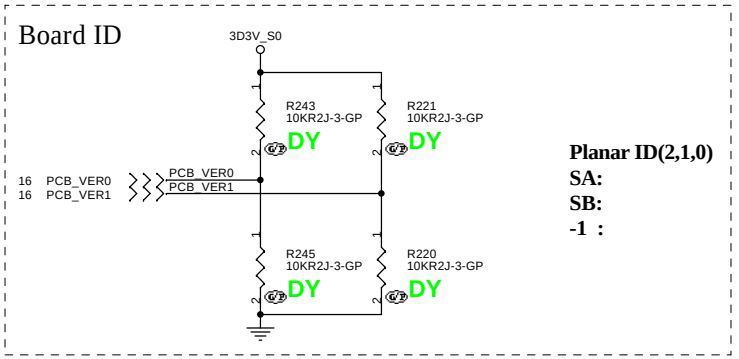
ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0



Planar ID(2,1,0)
SA:
SB:
-1 :

<Core Design>

Wistron Corporation
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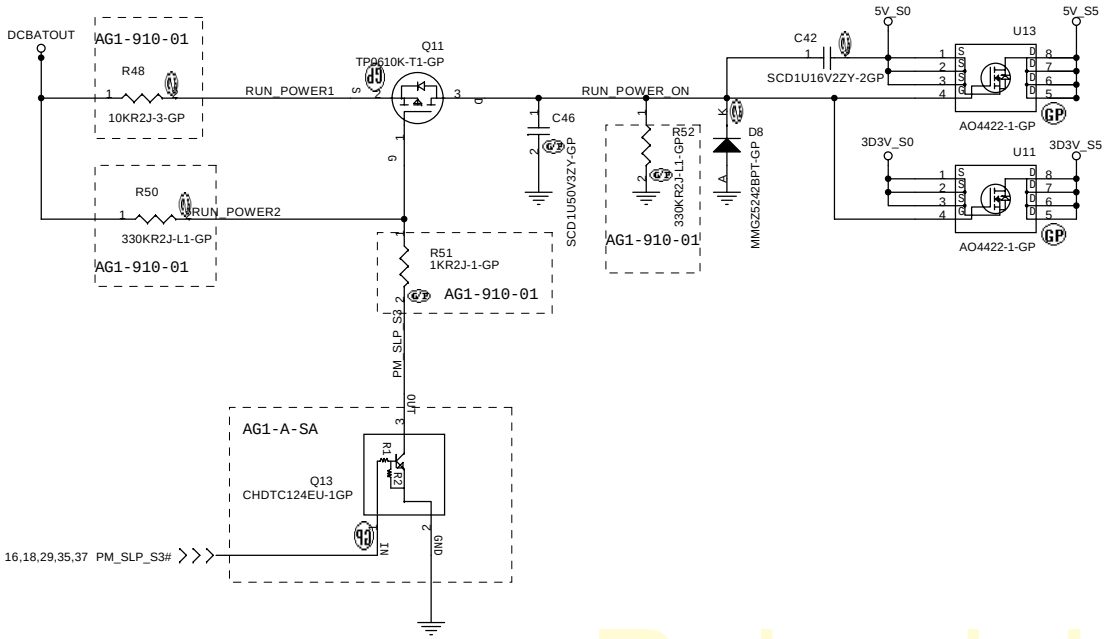
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS ROM**

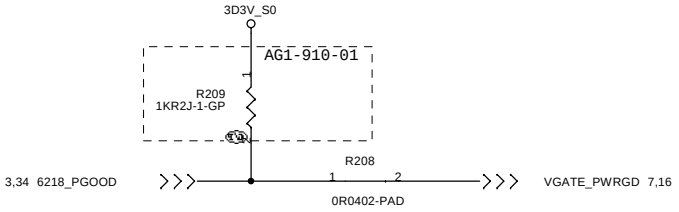
Size: A3 | Document Number: **AG1-910** | Rev: **01**

Date: Tuesday, November 01, 2005 | Sheet 31 of 40

Run Power



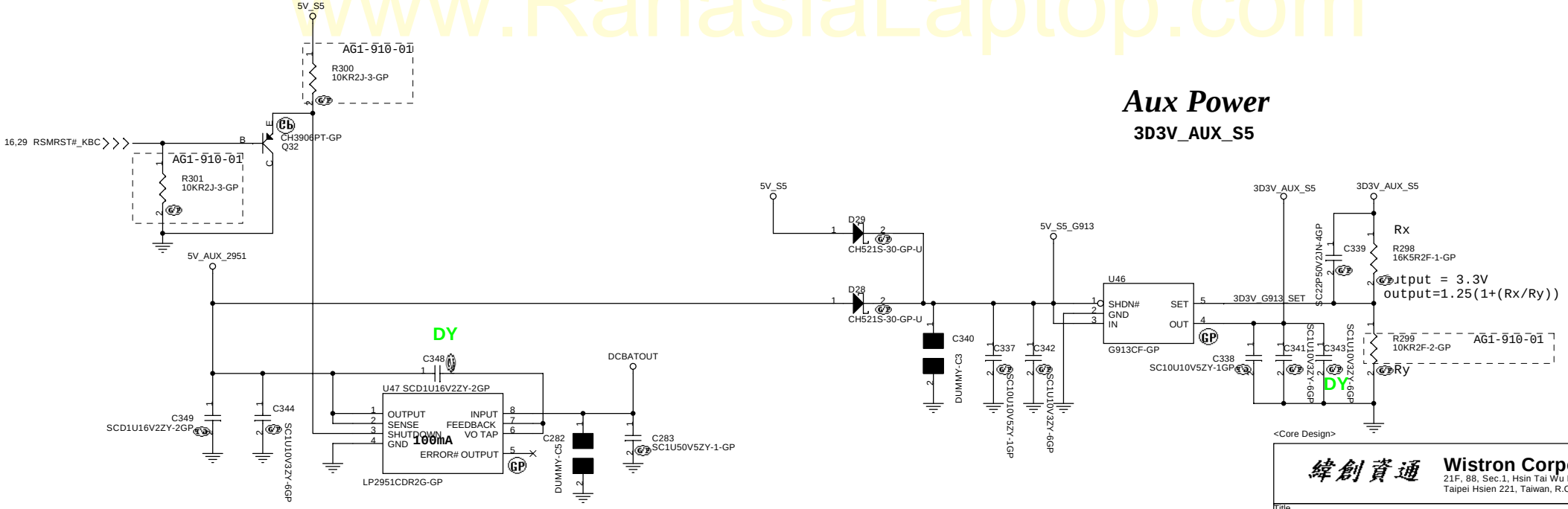
PWRGD for NB and SB



PWRGD to Turn on CPU_Core_Power

Aux Power

3D3V_AUX_S5



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

Size	Document Number	Rev
A3	AG1-910	01

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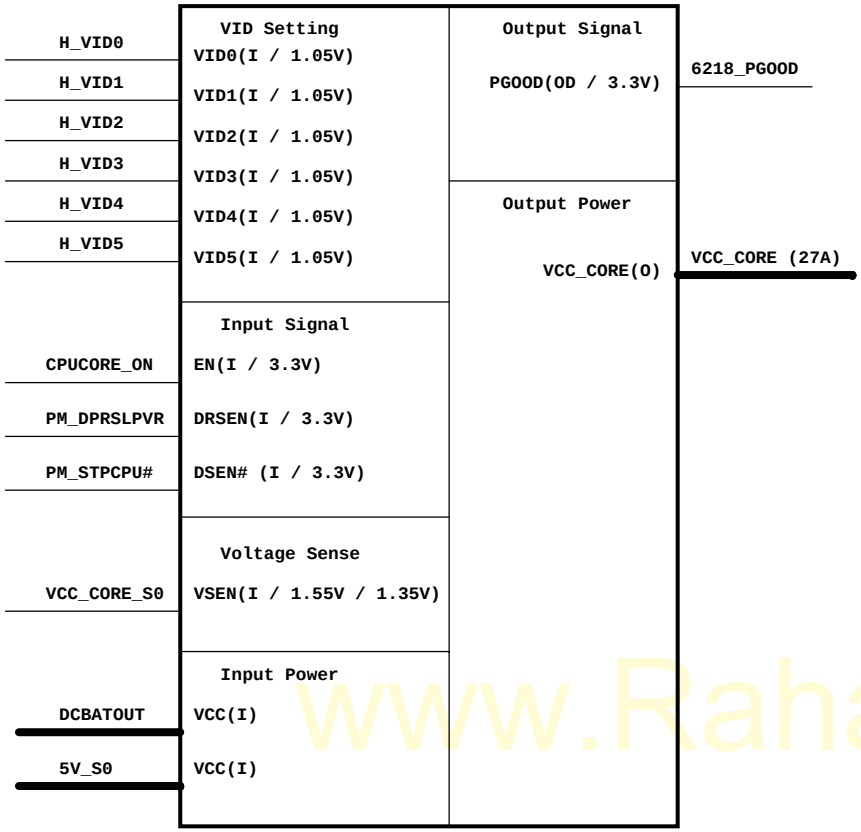
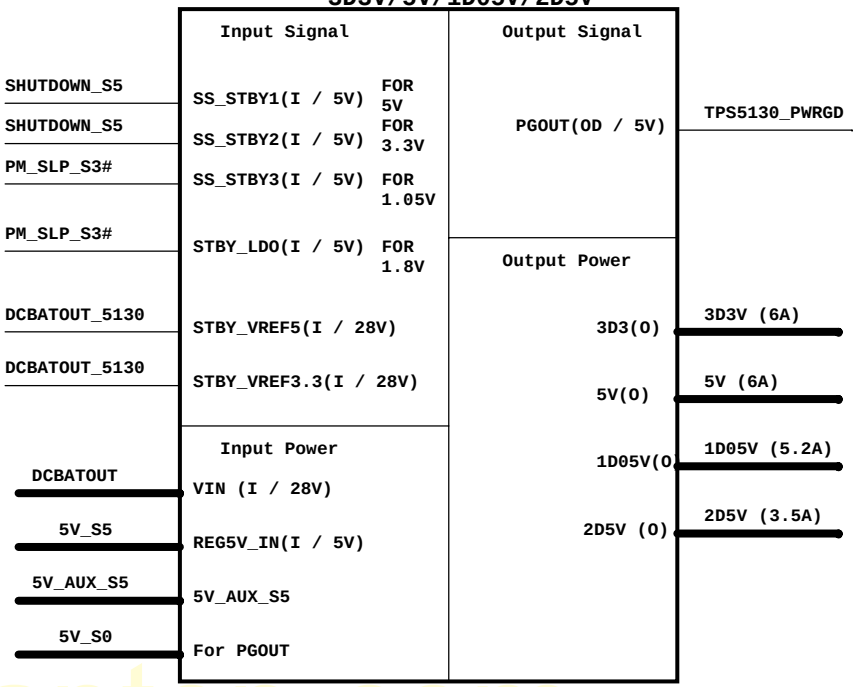
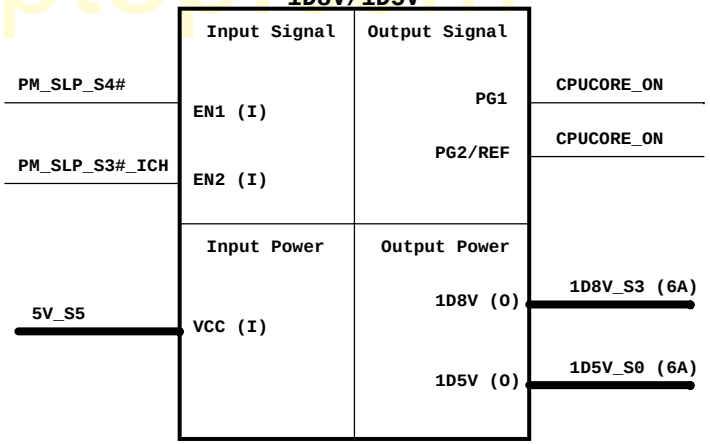
CPU_CORE ISL6218CV



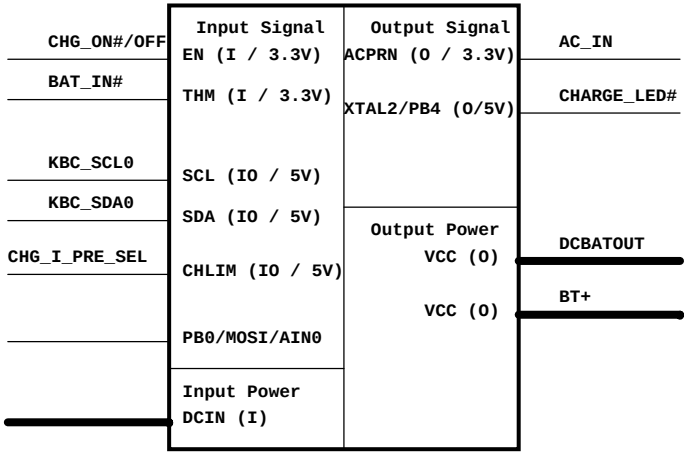
TPS5130 3D3V/5V/1D05V/2D5V



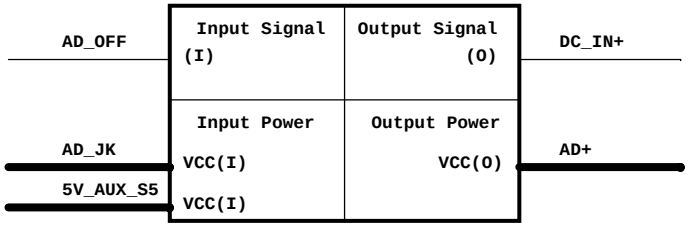
ISL6227 1D8V/1D5V



Charger_ISL6255



Adapter



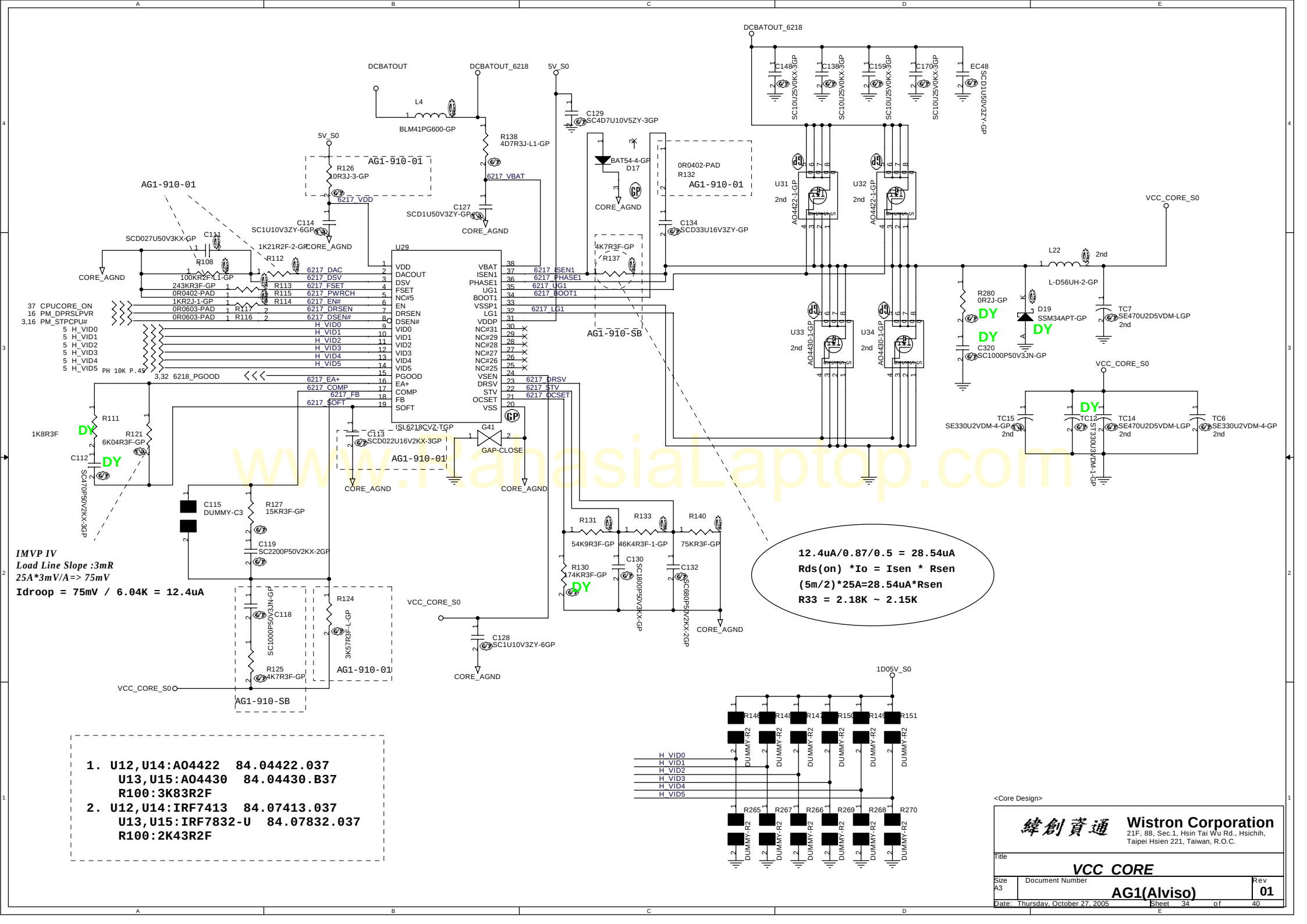
<Core Design>

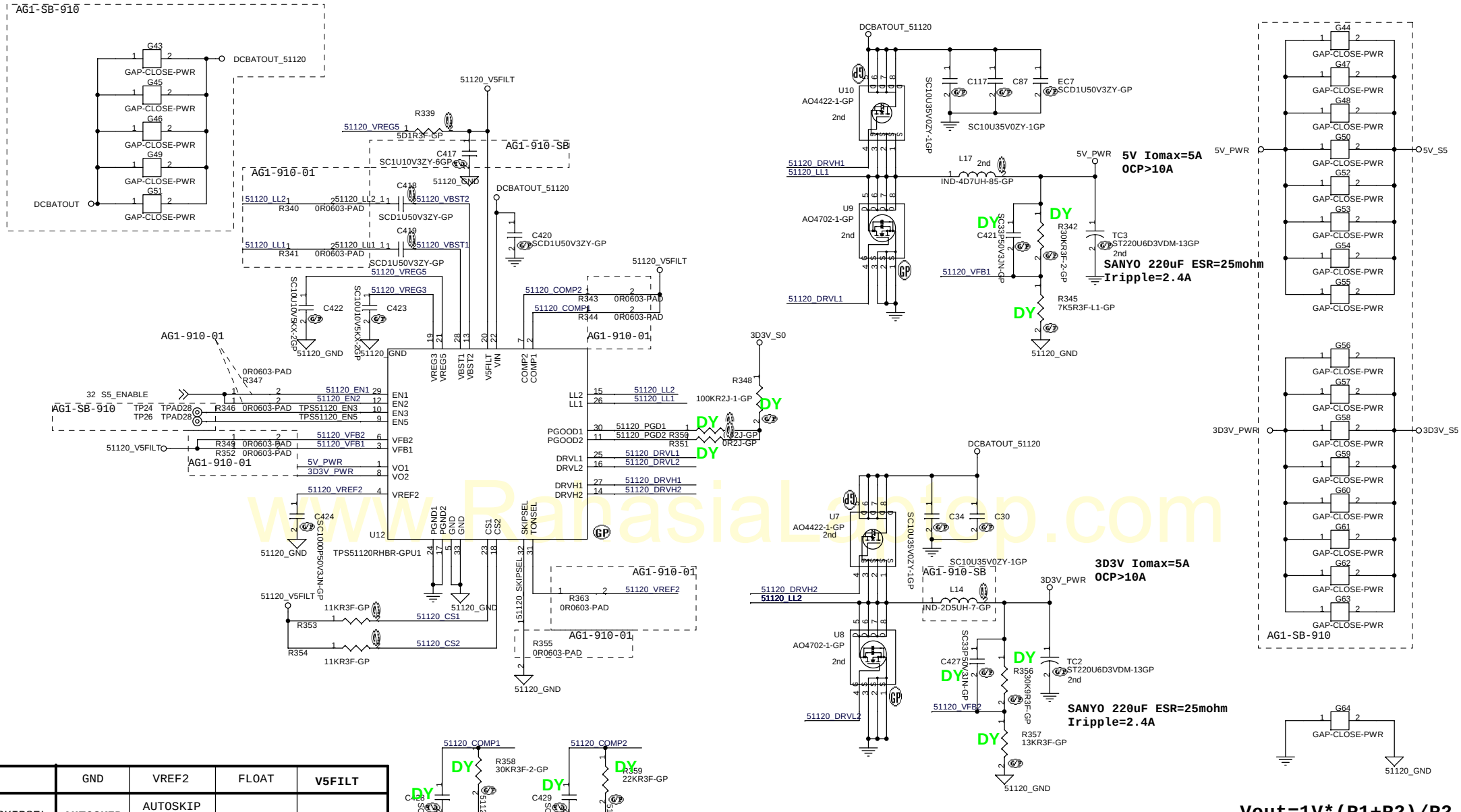
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Diagram***

Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Monday, October 17, 2005 Sheet 33 of 40





	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

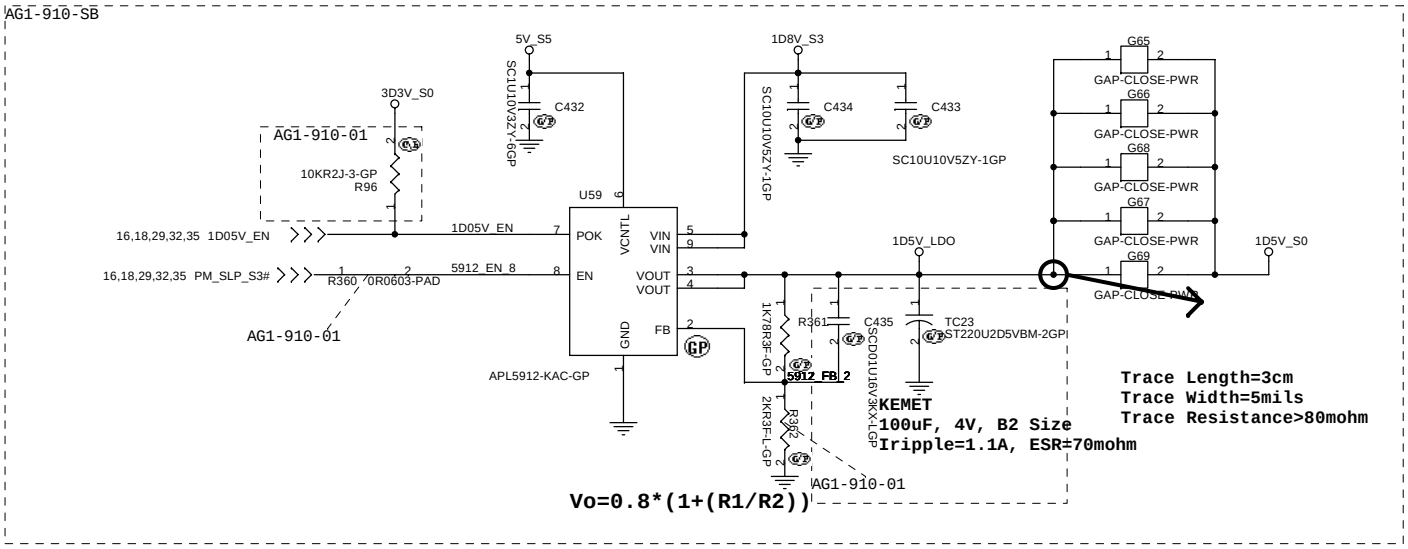
<Core Design>

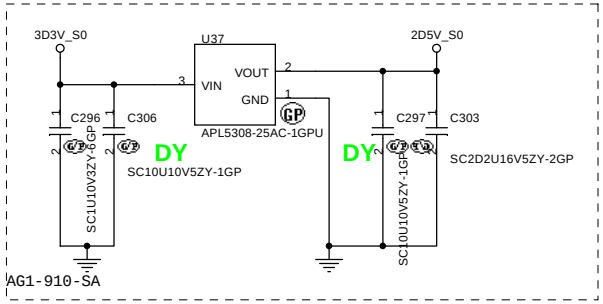
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51120 3D3V 5V***

Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Friday, October 28, 2005 | Sheet 35 of 40





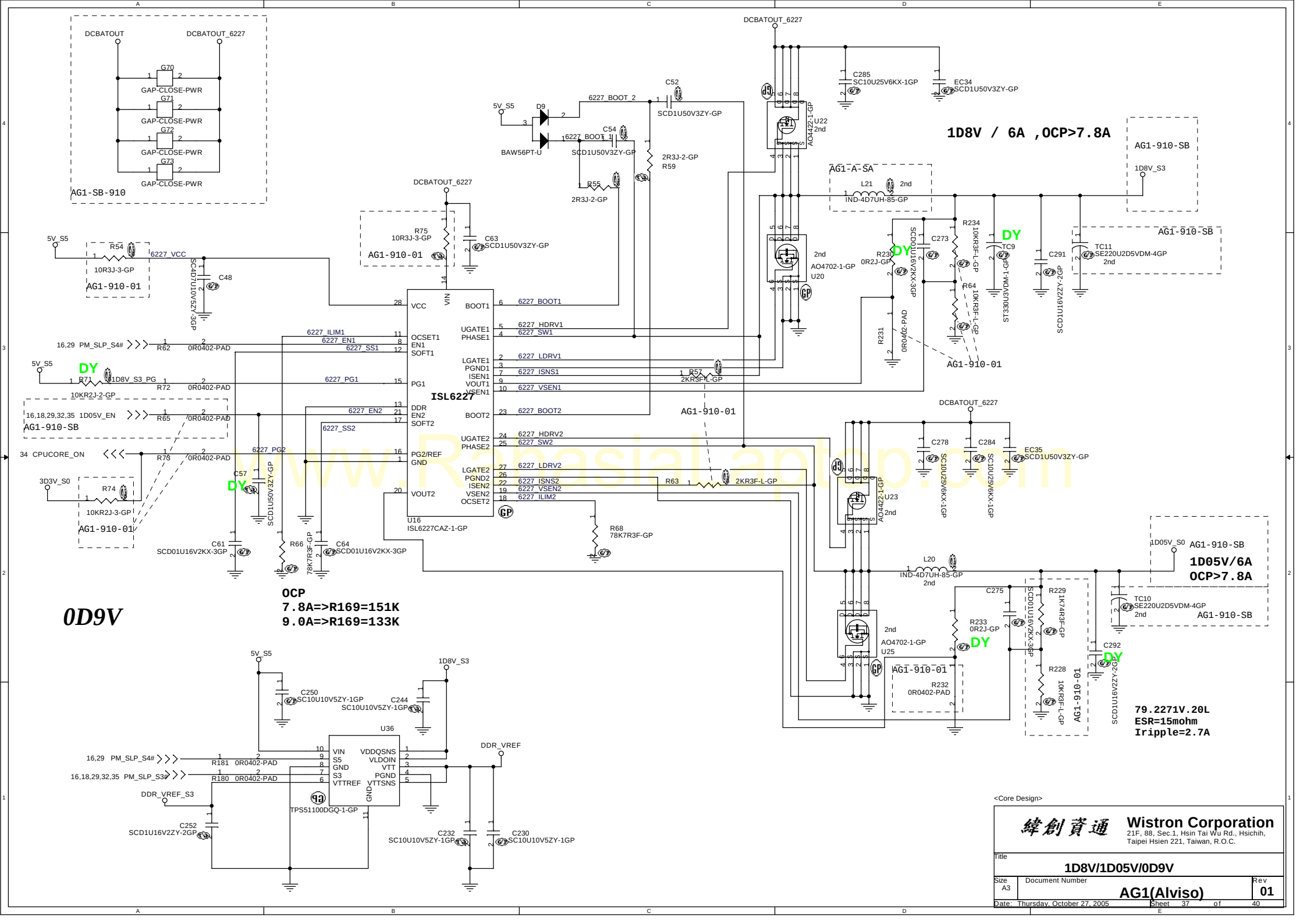
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D5V/2D5V(LDO)

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

Date: Monday, October 31, 2005 | Sheet 36 of 40


DCBATOUT
DCBATOUT_6227
G70
G71
G72
G73
GAP-CLOSE-PWR
AG1-SB-910
1D8V / 6A ,OCP>7.8A
AG1-910-SB
1D8V_S3
AG1-A-SA
L21
IND-4D7UH-85-GP
ISL6227
U16
ISL6227CAZ-1-GP
AO4422-1-GP
AO4702-1-GP
U20
U22
U23
U25
1D05V/6A
OCP>7.8A
0D9V
OCP
7.8A=>R169=151K
9.0A=>R169=133K
79.2271V.20L
ESR=15mohm
Iripple=2.7A
U36
TPS51100DGQ-1-GP
DDR_VREF
DDR_VREF_S3
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1D8V/1D05V/0D9V
Size
A3
Document Number
AG1(Alviso)
Rev
01
Date: Thursday, October 27, 2005
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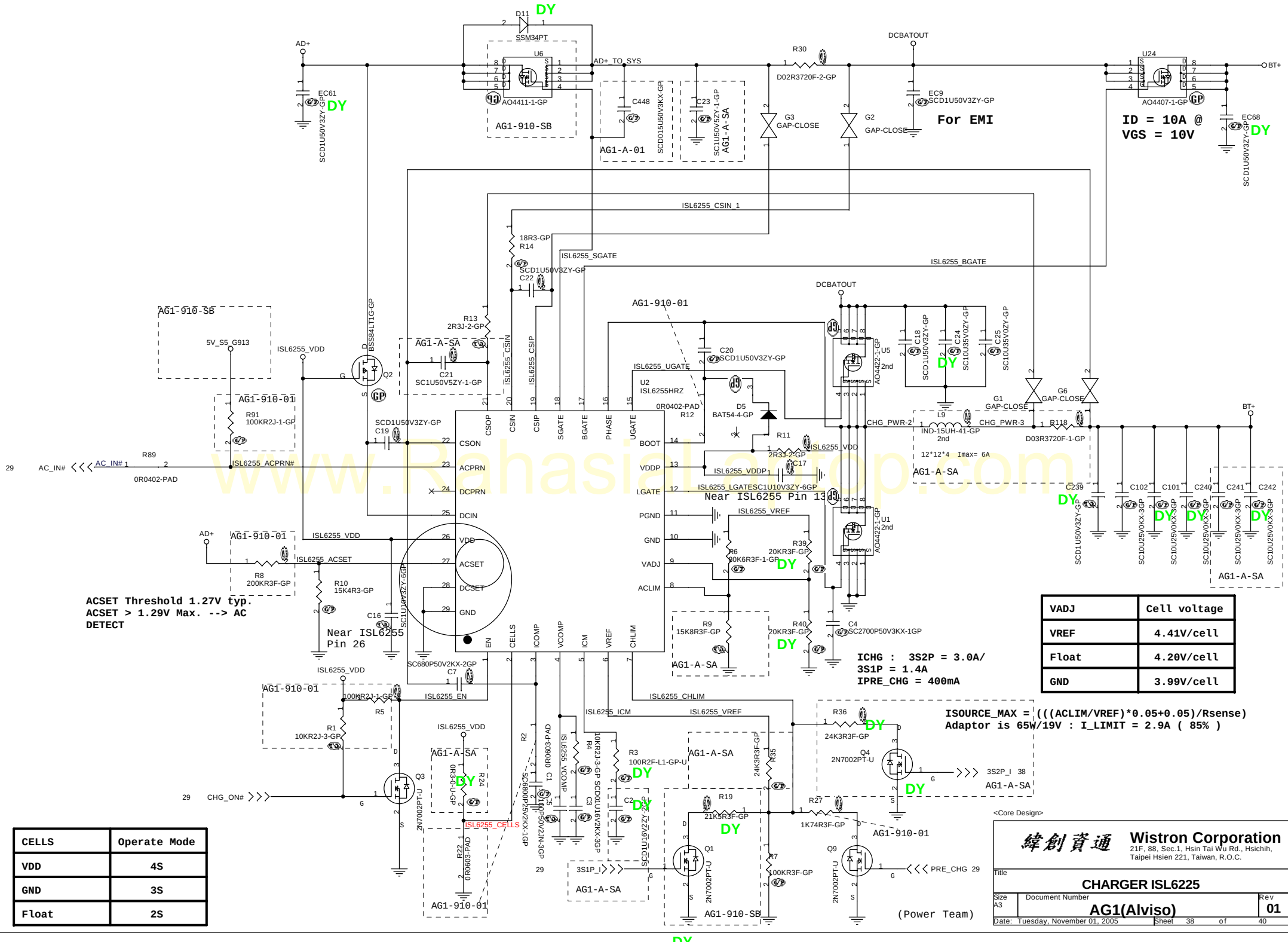

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6225

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

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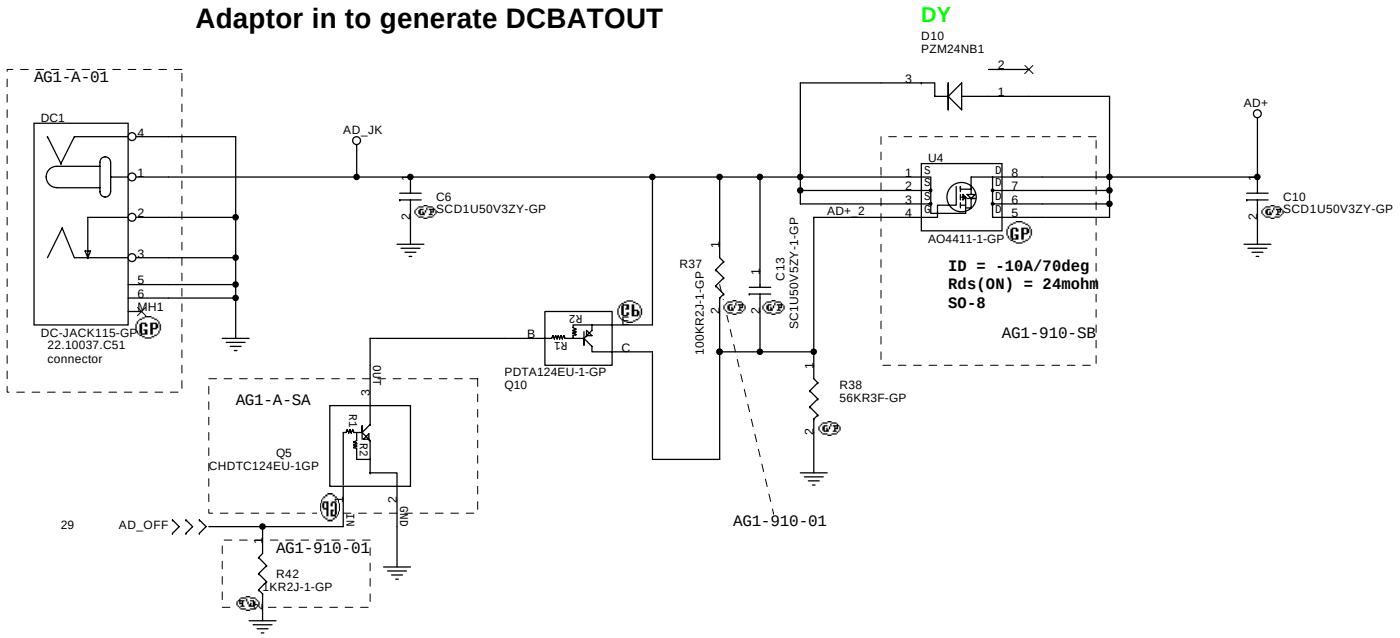
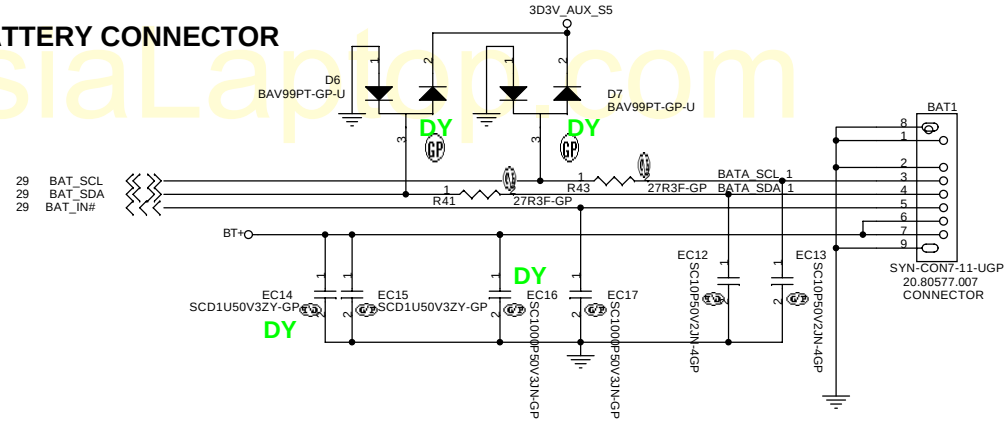
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

Wistron Corporation
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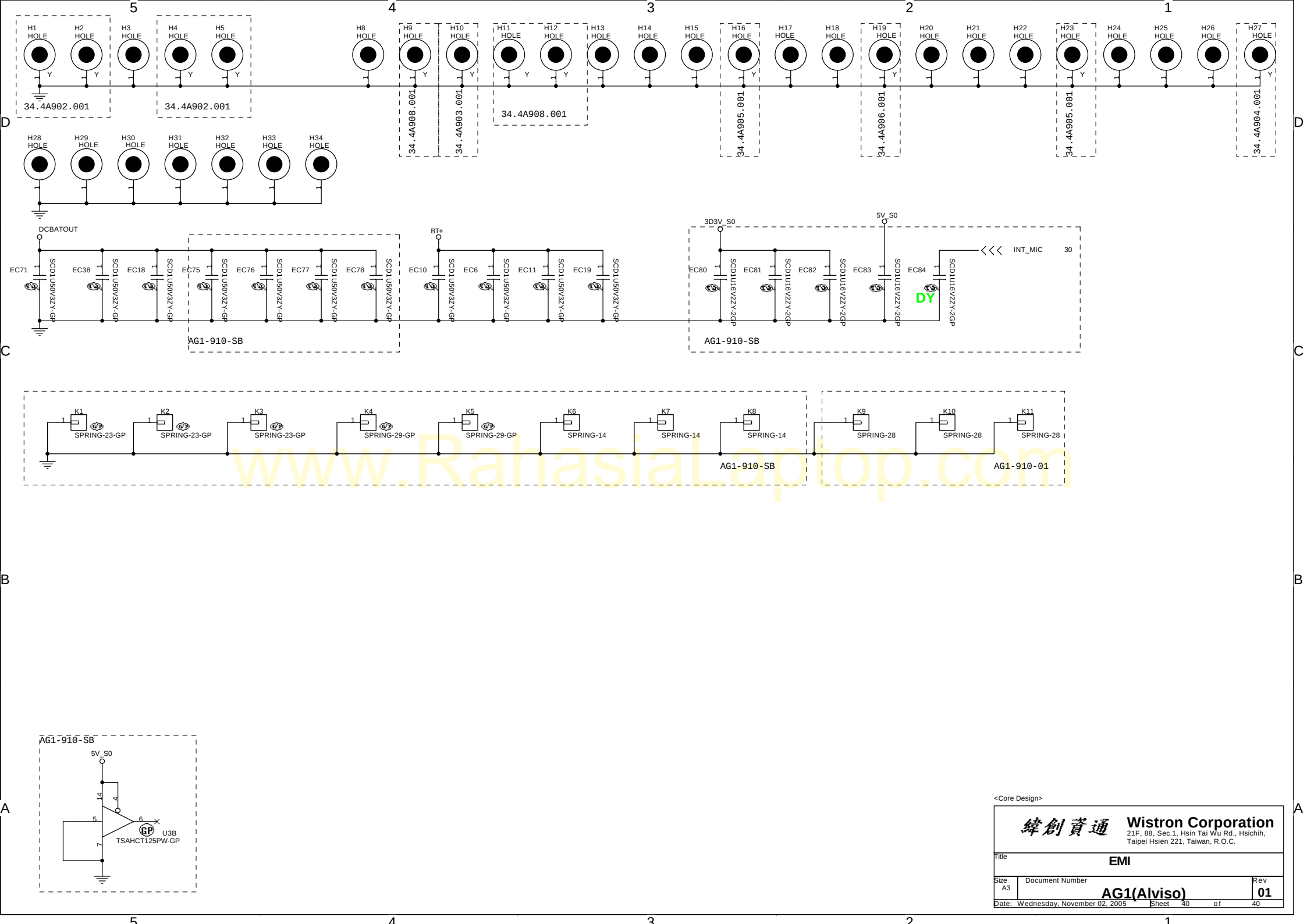
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

Date: Tuesday, November 01, 2005 | Sheet 39 of 40



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI**		
Size: A3	Document Number: **AG1(Alviso)**	Rev: **01**
Date: Wednesday, November 02, 2005	Sheet 40 of 40	